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GUVI

Global Ultraviolet Imager
Critical Design Review



Electronics Control Unit (ECU)

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GUVI ECU

- Design goals:
 - Increase performance over SSUSI Support Module to meet science requirements for GUVI
 - Improve instrument performance and testability by incorporating additional electrical functions in the ECU
 - Minimize development cost by leveraging TIMED IEM design parameters
 - Increase performance and flexibility of the power system by replacing the SSUSI Power Converter with new APL design
 - Improve packaging to reduce weight and complexity



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GUVI ECU

- Environmental requirements:
 - Random Vibration
 - Overall level = 17 grms, 1 minute per axis
 - Radiation
 - Total dose < 5 krads
 - No SEU can impact mission and no latch-up permitted
 - Temperature
 - Flight operational: Baseplate -24 to +55 °C
 - Test range: Baseplate -24 to +55 °C
 - Survival range: Baseplate -29 to +60 °C



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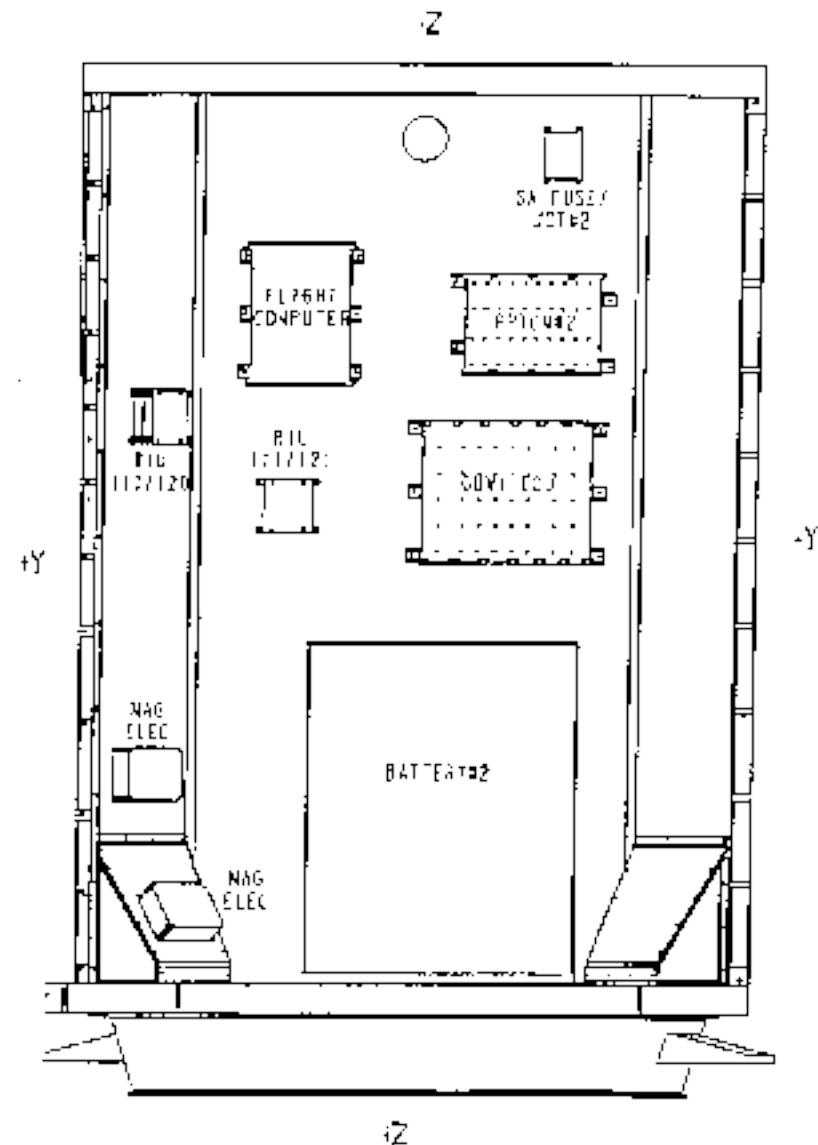
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S/C Configuration

- ECU located on -X panel internal to S/C
- SIS located on +Z deck (nadir-looking)
- Max cable length = 6 feet
- Cable way thru +Z deck
- ECU mass = 6.14 Kg.





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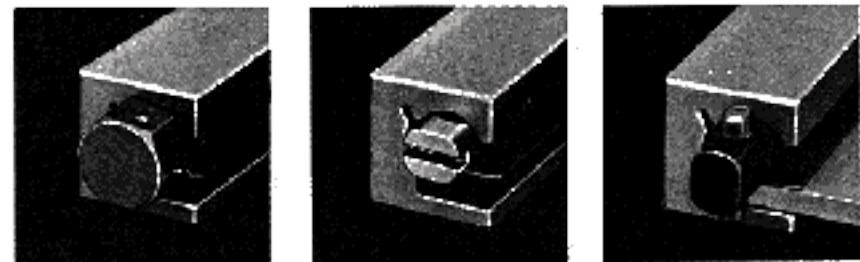
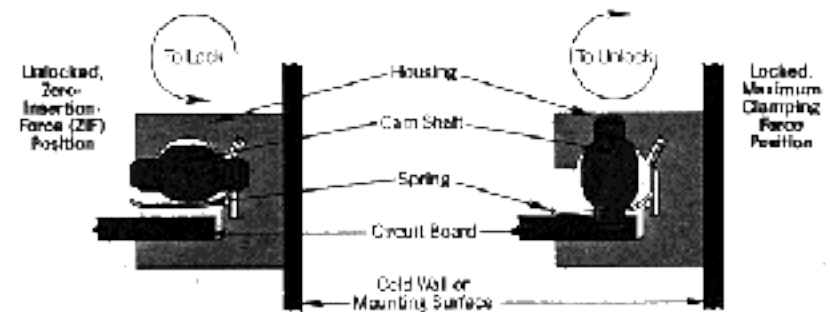
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ECU Chassis Card Locks

- IERC ZIF retainer
w/ stainless steel rod/cam assy
- Good thermal conduction
- No sticking problems
- Tolerance issues resolved:
TSM-97-110, 11 Dec. 1997





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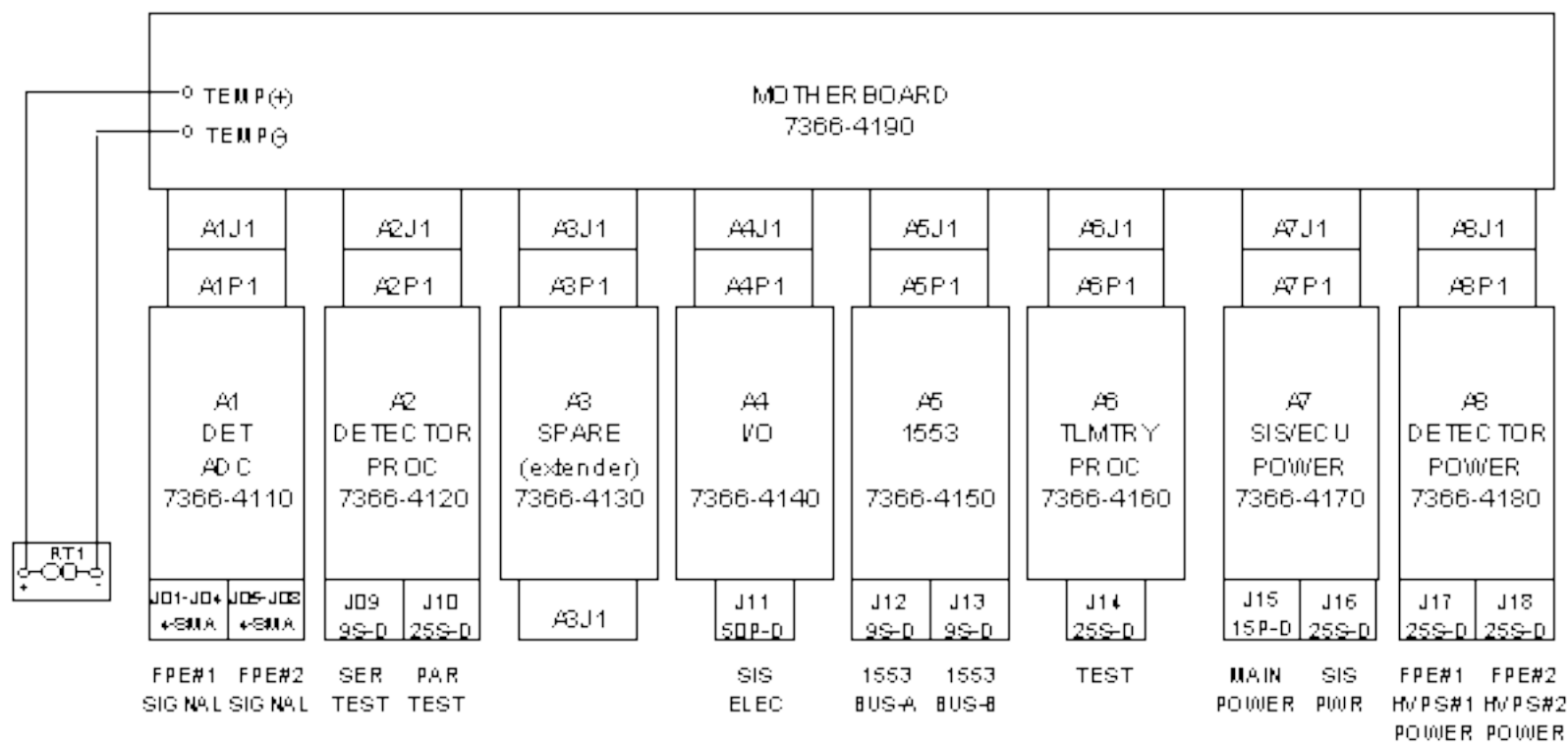
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ECU BLOCK DIAGRAM

EBA 12/11/97



NOTE: Heater power & S/C temperature connections go directly to the SIS.
FPE digital signal connections are within ECU due to location of Det ADC board.



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GUVI ECU Boards

- Detector ADC - APL Engineering design
- Detector Processor - APL BB, schematic done
- Extender - APL In fab
- I/O - Aerospace DM engineering test
- 1553 - Aerospace DM engineering test
- Telemetry Proc. - Aerospace DM engineering test
- SIS/ECU Power - APL In fab
- Detector Power - APL In fab
- Motherboard - APL DM engineering test



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ECU Changes Since PDR

- Design improvements to meet science requirements:
 - **ADC board**
 - **Detector Processor**
- HVPS control options on Detector Power board
- S/C power entry connector and filtered backplane connector on SIS/ECU Power board
- Orientation of backplane connector for Detector Power board
- Backplane signal names



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GUVI ECU Motherboard

- Layering scheme (12 layer PCB):
 - 1 Primary side Signal_1 Pad_1
 - 2 Ground plane Power_1
 - 3 Internal signal 1 Signal_2
 - 4 +15V_ECU plane Power_2
 - 5 Internal signal 2 Signal_3
 - 6 +5V_ECU plane Power_3
 - 7 Ground plane Power_4
 - 8 Internal signal 3 Signal_4
 - 9 -15V_ECU plane Power_5
 - 10 Internal signal 4 Signal_5
 - 11 Ground plane Power_6
 - 12 Secondary side Pad_2 Signal_6



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GUVI ECU Motherboard Status

- Circuit design finished and schematic complete
- DM artwork placement and routing complete
- DM boards fabricated and in engineering test
- Assembly drawing complete
- Flight parts in stock



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GUVI ECU Extender Board

- Layering scheme (10 layer PCB):
 - 1 + 5V return plane
 - 2 Signal 1
 - 3 + 5V plane
 - 4 Signal 2
 - 5 $\pm 15V$ return split planes
 - 6 $\pm 15V$ split planes
 - 7 Signal 3
 - 8 + 5V return plane
 - 9 Signal 4
 - 10 + 5V return plane



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GUVI ECU Extender Board Status

- Mechanical ICD complete
- Design finished and schematic complete
- Artwork placement and routing complete
- Level 1 boards in fabrication
- Assembly drawing complete
- Parts in by 2/1/98



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GUVI ECU Power Boards

- Design goals:
 - Minimize cost and development time by using standard high-rel "off-the-shelf" hybrid DC/DC converters with MIL-STD-883 screening.
 - Leverage TIMED IEM power board designs and NEAR designs:
 - **No duplication of effort for component qualification**
 - **Circuit reuse**
 - **Focus on unique requirements**



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GUVI ECU Power Boards

- QA Requirements:
 - MIL-STD-1772 Certified facility preferred
(requirements for hybrid facility & production line)
 - MIL-STD-38534 Certified
(requirements for element evaluation, process control, device screening, inspections, etc. of hybrid manufacturing), Class H parts with MIL-STD-883 test methods and PIND, XRAY, Pre-cap inspections)



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GUVI ECU Power Boards

- Input Electrical Requirements:
 - Operational Input voltage: 22 to 35 V
 - Operational input voltage transients : 22 to 35V and 35 to 22V in <5ms
 - Survival Input voltage: 0 to 22 V and 35 to 40 V
 - Survival input voltage transient: drop-out down to 0V for 2 to 50ms (rise and fall time <2ms) then up to 40V for 50ms
 - Conducted susceptibility: Survive CS01-02 2Vpp 10Hz to 400MHz, CS06 56V for 10uS per Mil-STD-461, 462
 - Conducted Emissions: CE01-03 per 7363-9038 TIMED EMI/EMC spec
 - Inrush current: < 2.5A peak after first 10uS (at relay turn ON)
 - Slow input voltage ramp up: Bench testing, no instabilities allowed



GUVI ECU Power Boards

- Output Electrical Requirements: (for hybrid DC/DC converters)
 - Line regulation: $\pm 1\%$
 - Load regulation: $\pm 1\%$
 - Cross regulation: $\pm 3\%$ (Loading of cross regulated outputs are within 30% of each other)
 - Switching Ripple: $< 100 \text{ mVpp}$ (550kHz)
 - Switching Spike: $< 150 \text{ mVpp}$ (10MHz)
 - Step load response: $\pm 3\%$ (20% of full load step)
 - Input transient response: $\pm 2\%$
 - Efficiency (28Vin): $\geq 75\%$ at max rated load
 - Output voltage survival overshoot, 15ms duration: 3.3V=4.125V, 5V=6.25V, 9V= 11.25V, 12V= 15V, 15V= 18.75V



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GUVI ECU Power Boards

- Converter Evaluations:
 - Result in 2 families: Lambda Advanced Analog (LAA) and Interpoint both meet environmental requirements after extensive testing
 - Both have the same footprint, pin-outs, and output power levels
 - LAA shows improved electrical performance:
 - step loads (ATR vs MTR)
 - no output overshoot
 - reduced switching noise (> 2 MHz)
 - Baseline design uses LAA devices with Interpoint as a backup



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- Lambda Advanced Analog converters:
 - AHF2805S 2.4A @ 5V 12W max
 - AHF2815D 0.8A @ $\pm 15V$ 12W max
 - ATR family 30W max
 - AFV461 EMI filter 4A @ 40V
- Interpoint converters:
 - MHF+2805S
 - MHF+2815D
 - MTR family
 - FMC461 EMI filter



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Power Requirements

OUTPUT VOLTAGE (NOMINAL) (VDC)	MIN LOAD CURRENT (mA)	AVG LOAD CURRENT (mA)	MAX LOAD CURRENT (mA)	MAX POWER (mW)	MAX OUTPUT RIBBLE & NOISE (mV p-p)	MIN OUTPUT VOLTAGE (VDC)	MAX OUTPUT VOLTAGE (VDC)	SUBSYSTEM
+6.00 (fr +1.5)	94	94	94	1440	60	5.90	6.20	FPE 1
-6.00 (fr -1.5)	38	38	38	570	60	-6.30	-5.70	FPE 1
+6.00 (fr +1.5)	94	94	94	1440	60	5.90	6.20	FPE 2
-6.00 (fr -1.5)	38	38	38	570	60	-6.30	-5.70	FPE 2
+28.00	7	40	40	1120	150	26.60	29.40	HVPS 1
+28.00	7	40	40	1120	150	26.60	29.40	HVPS 2
				6240	DETECTOR POWER BOARD			
+5.00	30	55	55	275	50	4.75	5.25	SE
+20.00	0	200	250	5000	200	18	22	SE
+5.00	140	140	220	1100	50	4.75	5.25	Det+ADC
	125	130	144	830	50	4.75	5.25	Is km Proc
	208	208	478	2390	50	4.75	5.25	1553 bd
	117	117	117	585	50	4.75	5.25	IO bd
	100	150	200	1000	50	4.75	5.25	DetProc
+15.00	15	15	15	225	150	14.25	15.75	IO bd
	20	20	20	300	150	14.25	15.75	Det+ADC
-15.00	30	30	30	450	150	-15.75	-14.25	IO bd
	20	20	20	300	150	-15.75	-14.25	Det+ADC



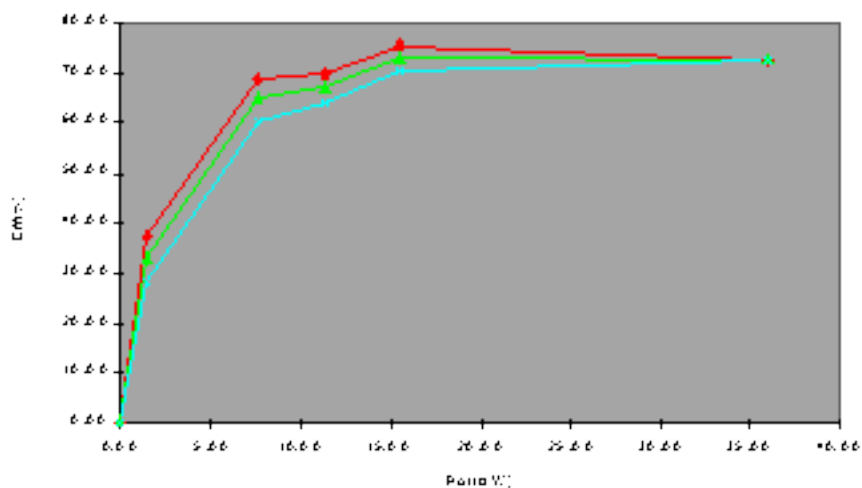
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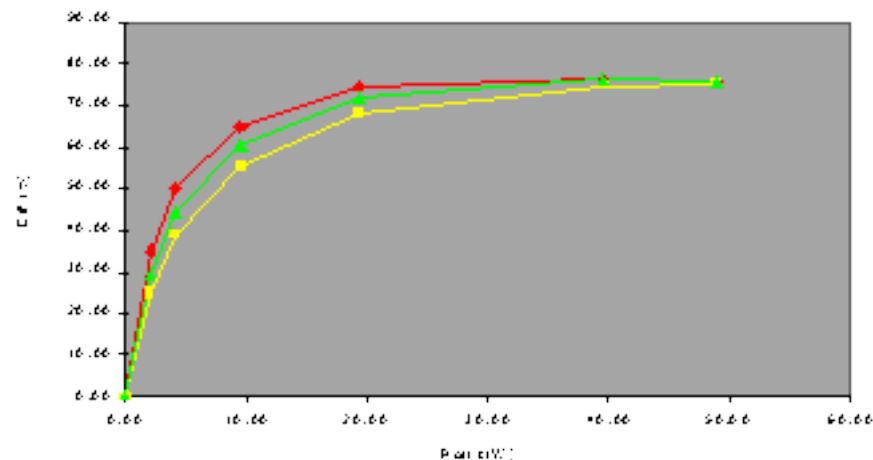
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WTR/Downlink Power Conv BB Efficiency
(Vin=22,28 & 36V)



ROVR/Uplink Power Conv BB Efficiency
(Vin=22,28 & 36V)



Power Converter BB Efficiency Measurements (from D.K. Temlin)



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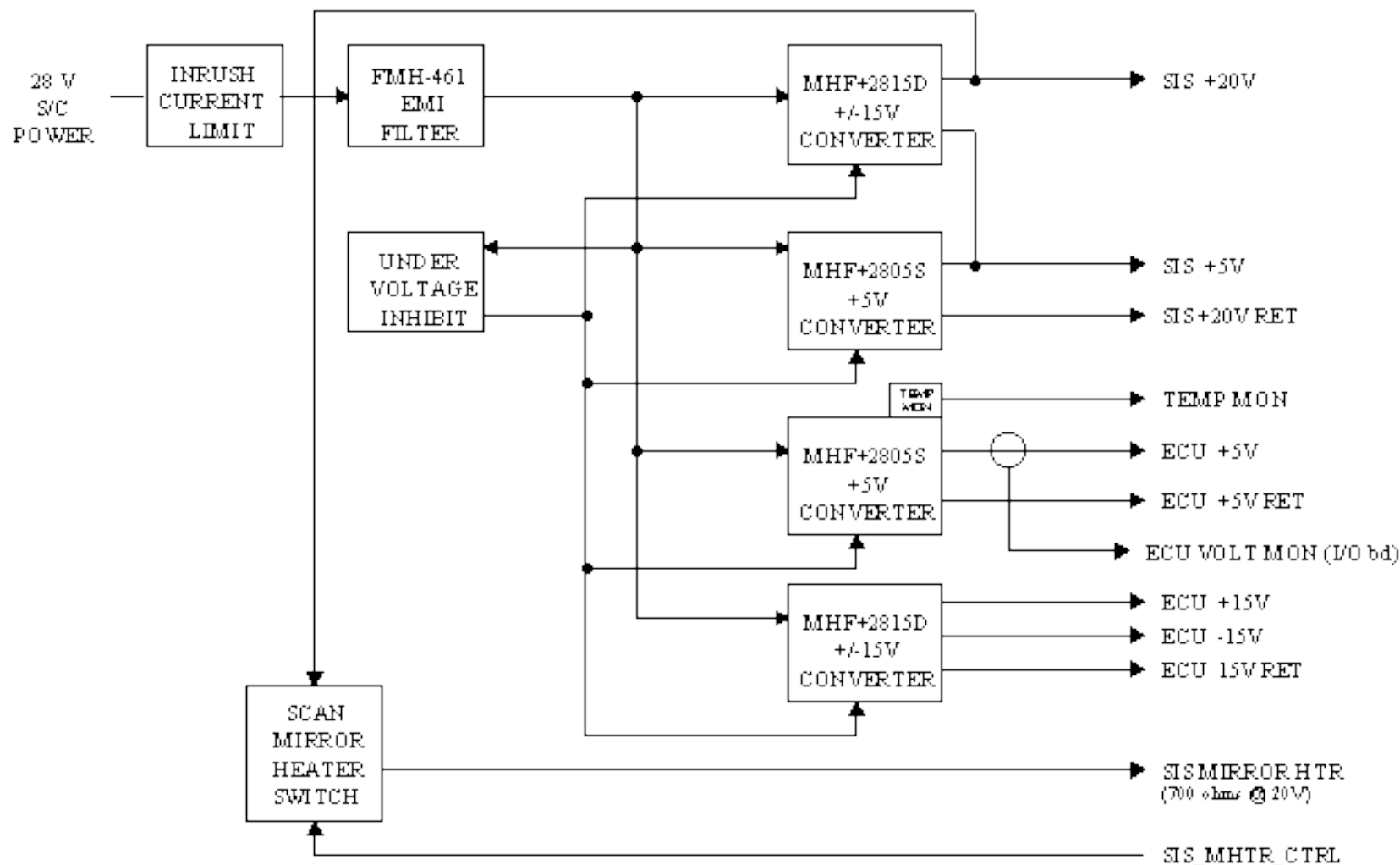


GUVI ECU Power Boards

- Existing Design:
 - Inrush current limit
 - Input under voltage lockout
 - Current monitor
 - Power switching for primary & secondary detectors
- Custom Design:
 - Scan mirror operational heater power control
 - $\pm 6V$ output for FPEs
 - + 28V output for HVPS control
 - + 20V output for scan motor operation



SIS/ECU POWER BOARD BLOCK DIAGRAM



5 BUCKS
TOTAL POWER = 12.5 W (supplied) + 6.0 W (dissipated assuming 60% average efficiency)



GUVI ECU Power Boards

- Layering scheme (10 layer PCB):
 - 1 Ground plane
 - 2 +5V Power
 - 3 +5V Power
 - 4 Ground plane
 - 5 +15V Power
 - 6 +15V Power
 - 7 Ground plane
 - 8 -15V Power
 - 9 -15V Power
 - 10 Ground plane

> **Output trace fills**

> **Output trace fills**

> **Output trace fills**



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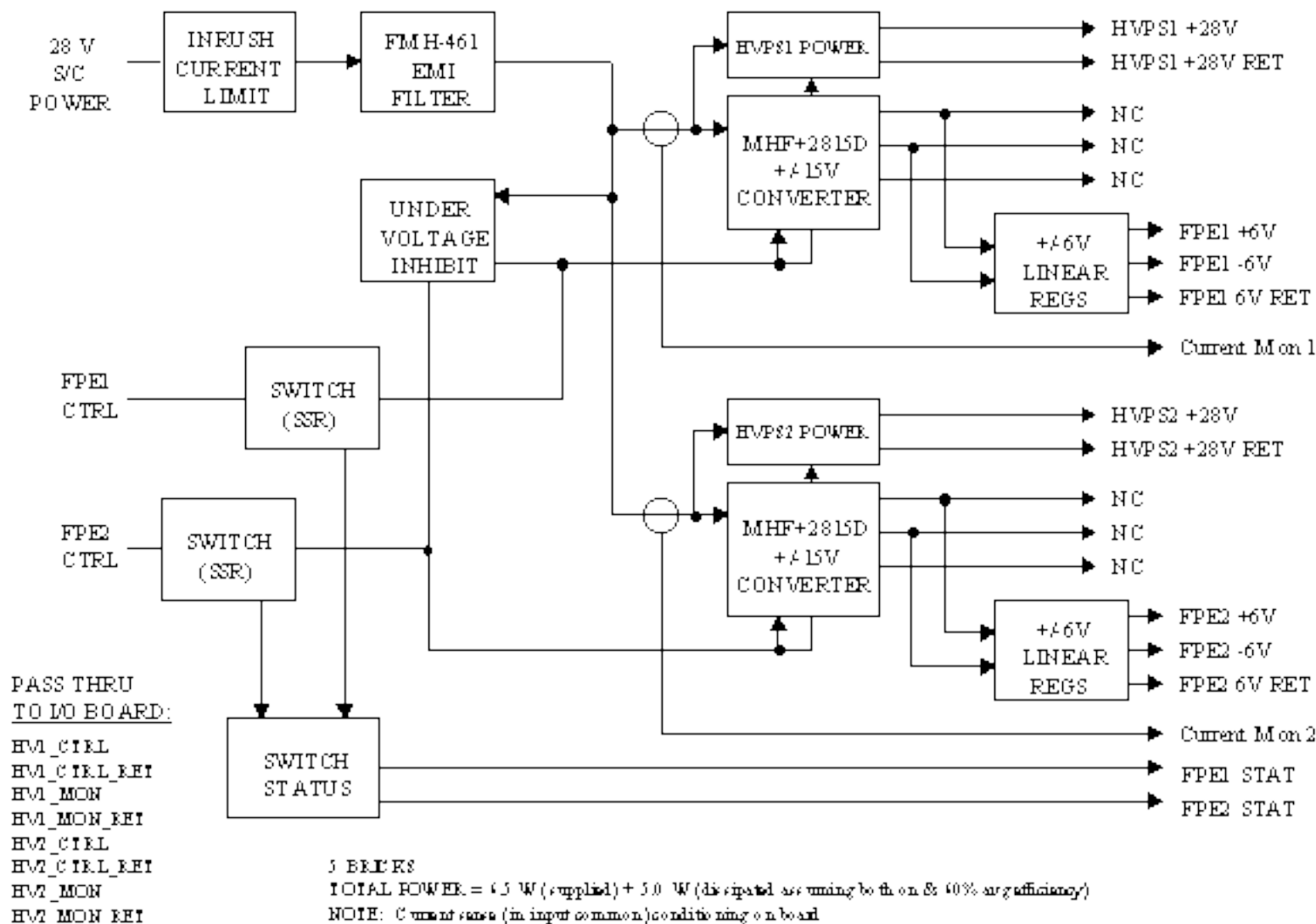


SIS ECU Power Board

- Status:
 - Circuit design finished and schematic complete
 - EDR to be held 1/16/98
 - DM artwork placement and routing complete
 - Heatsink and assembly drawings complete
 - DM parts in by 1/15/98
 - Flight parts in by 3/15/98



DETECTOR POWER BOARD BLOCK DIAGRAM





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Detector Power Board

- Status:
 - Circuit design finished and schematic complete
 - EDR to be held 1/16/98
 - DM artwork placement complete
 - DM artwork routing in progress
 - DM parts in by 2/1/98
 - Flight parts in by 3/15/98



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GUVI ECU Power Boards

- IEM Breadboard Test Measurements:
 - Inrush current
 - Output voltage during turn-on
 - Switching ripple
 - Step load response
 - CS01 input noise vs output ripple
 - CS06 input transient vs output response
 - Survival input voltage transient
 - CE-03 narrowband conducted emissions
- GUVI Boards Will Be Similarly Examined



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Schedule Summary

Description Drawing Number	DM Qty & (Planned date)	Design Complete (Planned date)	Electrical Design Data TSE-1	Data To PDM Released to TSE-2 (PWE)	Complete DM Board Basis (PWA)	DM Deliver to Engineer (PWA)	Complete Flight Board Basis (PWE)	Flight Qty Date Required	Late Flight Date Required
Electronic Control Unit									
BCU Detector ADC Bd 7366-4110	1 by 3/2/98	12/24/97	Schematic by 1/19/98	1/26/98	2/27/98	1 by 3/16/98	4/27/98	1 by 5/18/98	6/2/98
BCU Detector Processor Bd 7366-4120	1 by 2/2/98	12/12/97	Schematic by 12/23/97 WW	1/15/98	2/16/98	1 by 3/13/98	4/27/98	1 by 5/18/98	5/28/98
BCU Spare Extender Bd (4L) 7366-4130	4 by 2/13/98	12/6/97	Schematic by 12/29/97	1/9/98	1/30/98	3 by 2/10/98 1 to Aero 2/10/98		4 by 1/9/98	1/9/98
BCU SIS/BCU Power Bd 7366-4170	1 by 2/16/98	1/6/98	Schematic by 12/19/97	1/9/98	2/6/98	1 by 2/9/98	5/4/98	1 by 5/18/98	5/25/98
BCU Detector Power Bd 7366-4180	1 by 2/27/98	12/23/97	Schematic by 12/15/98	1/23/98	2/20/98	1 by 2/25/98	5/4/98	1 by 5/18/98	5/20/98
BCU Motherboard (ML 10) 7366-4190	2 by 11/18/97	10/6/97	Complete	11/16/97	11/17/97	2 by 12/4/97 (1) Aero 11/20	4/6/98	1 by 4/20/98	5/13/98
BCU Chassis Assembly 7366-4000	1 by 11/4/97	3/24/98	2/13/98	Complete		Complete Sheet Metal		1 by 5/19/98	5/19/98
Focal Plane Electronics									
FPB Bias Housing Assembly 7366-4203	1 by							2 by	
FPB HV Bias PWA 7366-4240	1 by 12/23/97	8/22/97				1 by 2/1/98		2 by 4/29/98	5/22/98
FPB Pre Amp PWA 7366-4250	1 by 12/16/97	12/23/97				1 by 2/1/98		2 by 4/29/98	5/22/98
FPB Assembly 7366-4200	1 by 11/20/97	10/30/97						2 by 6/11/98	8/31/98