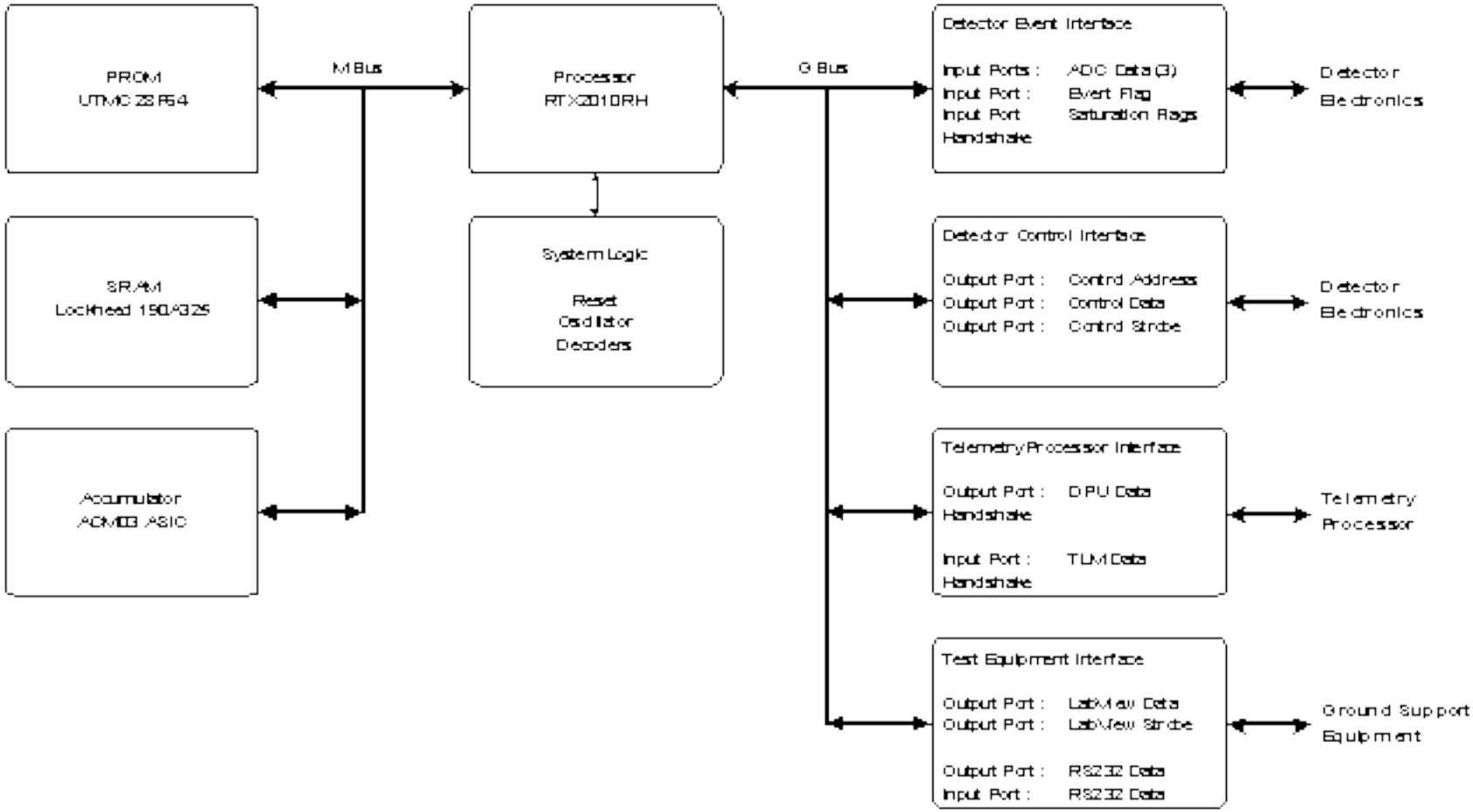
Detector Processor Hardware

J. D. Boldt

The Johns Hopkins University
Applied Physics Laboratory
Laurel, MD 20723-6099
Tel: (301) 953-5108
Fax: (301) 953-1093
E-Mail: john.boldt@jhuapl.edu

GUVI Detector Processor Hardware

Block Diagram



GUVI Detector Processor Hardware

Microprocessor

The DPU uses the Harris RTX2010RH microprocessor which has been used in many APL instruments...

- Cassini MIMI - particle instrument
- ACE ULEIS - particle instrument
- NEAR MSI - imager
- NEAR NIS - spectrograph
- NEAR MAG - magnetometer
- SSUSI - spectrographic imager

The RTX2010RH has features which make it a good choice for use in scientific instruments...

- Low power - CMOS SOS
- Radiation hardened - hard to 100 Krad total dose, latchup free
  - SEU immune (APL test)
- Compact design - single chip with minimal support logic required
- High performance - 6 MHz instruction cycle in the DPU
  - dual bus architecture allows multiple instructions per cycle
  - DPU design makes maximum use of the dual bus architecture

GUVI Detector Processor Hardware

Memory

The DPU uses two 8K*8 UTMC 28F64 PROM's for boot code storage.

- Low power - CMOS anti-fuse
- Fast access - 35 ns access allows zero wait state design
- Radiation hardened - hard to 100 Krad total dose, latchup free
  - SEU immune

The DPU uses two 128K*8 Lockheed Martin SRAM's for program execution and data buffering.

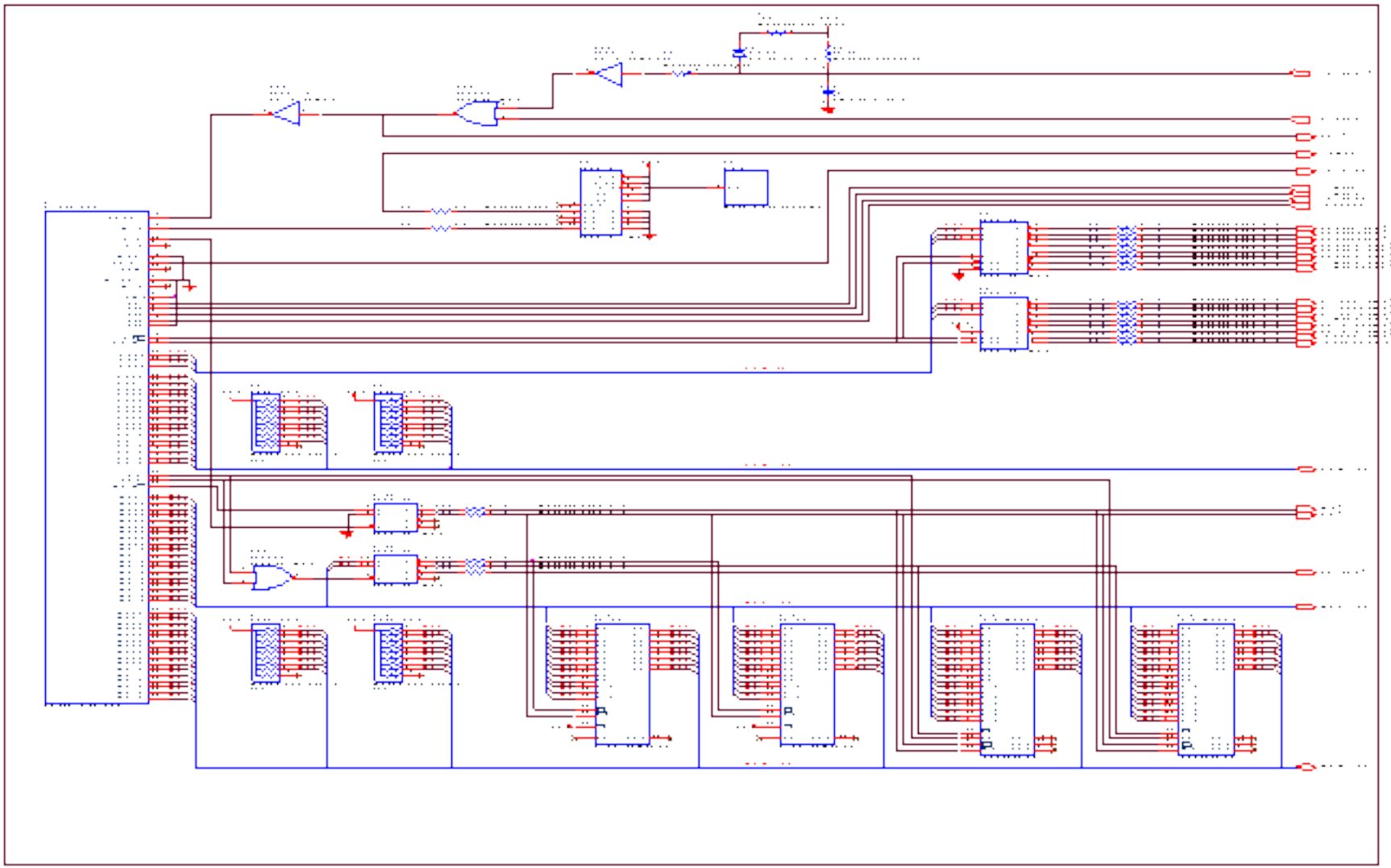
- Low power - CMOS
- Fast access - 40 ns access allows zero wait state design
- Radiation hardened - hard to 100 Krad total dose, latchup free
  - SEU rate < 1*10E-11 errors/bit-day

The DPU application code is downloaded into SRAM from the Telemetry Processor under control of the boot PROM code. The application code is executed from SRAM.

Discrete logic, as opposed to an FPGA, is used to interface memory to the microprocessor. Radiation tolerant AC logic from National Semiconductor allows zero wait state operation.

GUVI Detector Processor Hardware

Microprocessor and Memory



GUVI Detector Processor Hardware

Accumulator

The DPU uses one ACM03 accumulator chip to count detector events and to time event integration periods.

The ACM03 is a custom ASIC designed at APL by Nick Paschalidis and fabricated on a radiation hardened line at UTMC.

- Low power - CMOS
- Fast access - 20 ns access allows zero wait state design
- Radiation hardened - hard to > 1Mrad total dose, latchup free
- High performance - 16 counters (24 bit) and control logic in a single chip

Single event upset rates for a 90% worst case environment from Brookhaven testing...

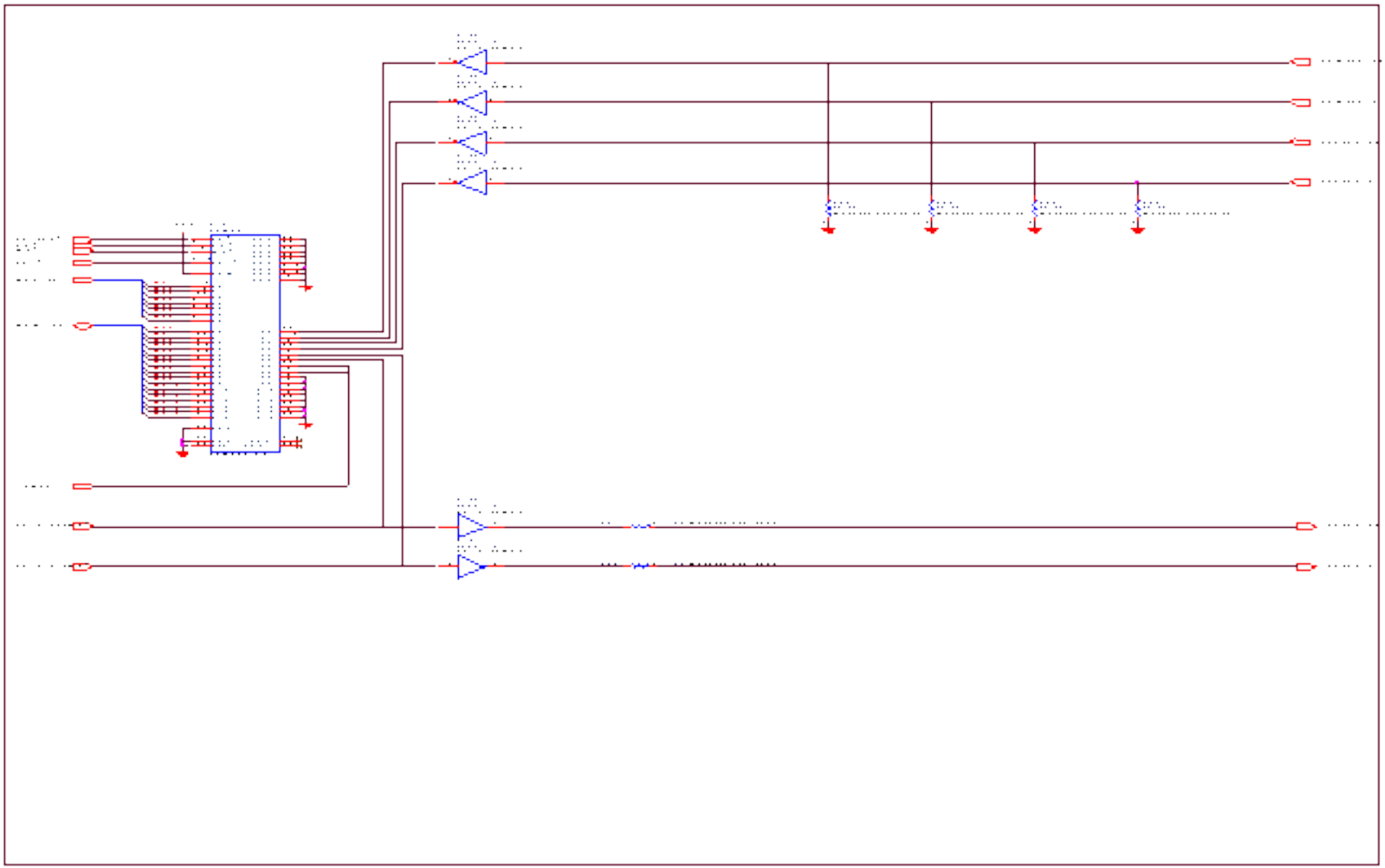
- Counters - 2.94*10E-6 errors/bit-day
- Mask registers - 8.20*10E-8 errors/bit-day

The DPU uses 8 of the 16 available counters. The expected overall single event upset rate for these 192 bits is one error per 4.85 years.

The ACM03 is currently being flown in the MIMI particle instrument as part of the Cassini mission to Saturn.

GUVI Detector Processor Hardware

Accumulator



GUVI Detector Processor Hardware

Detector Event Interface

The DPU receives detector events across the ECU backplane as three simultaneous 12-bit words. The words are latched into DPU registers by a simple handshake with the detector electronics.

The DPU microprocessor polls for detector events on a "1-bit" input port. The other 15 bits on the input port are forced to zeros. The additional hardware of the "1-bit" input port improves DPU throughput by making use of the RTX2010RH microprocessor's ability to set the zero flag during reads, allowing the software to avoid the overhead of additional mask and compare instructions.

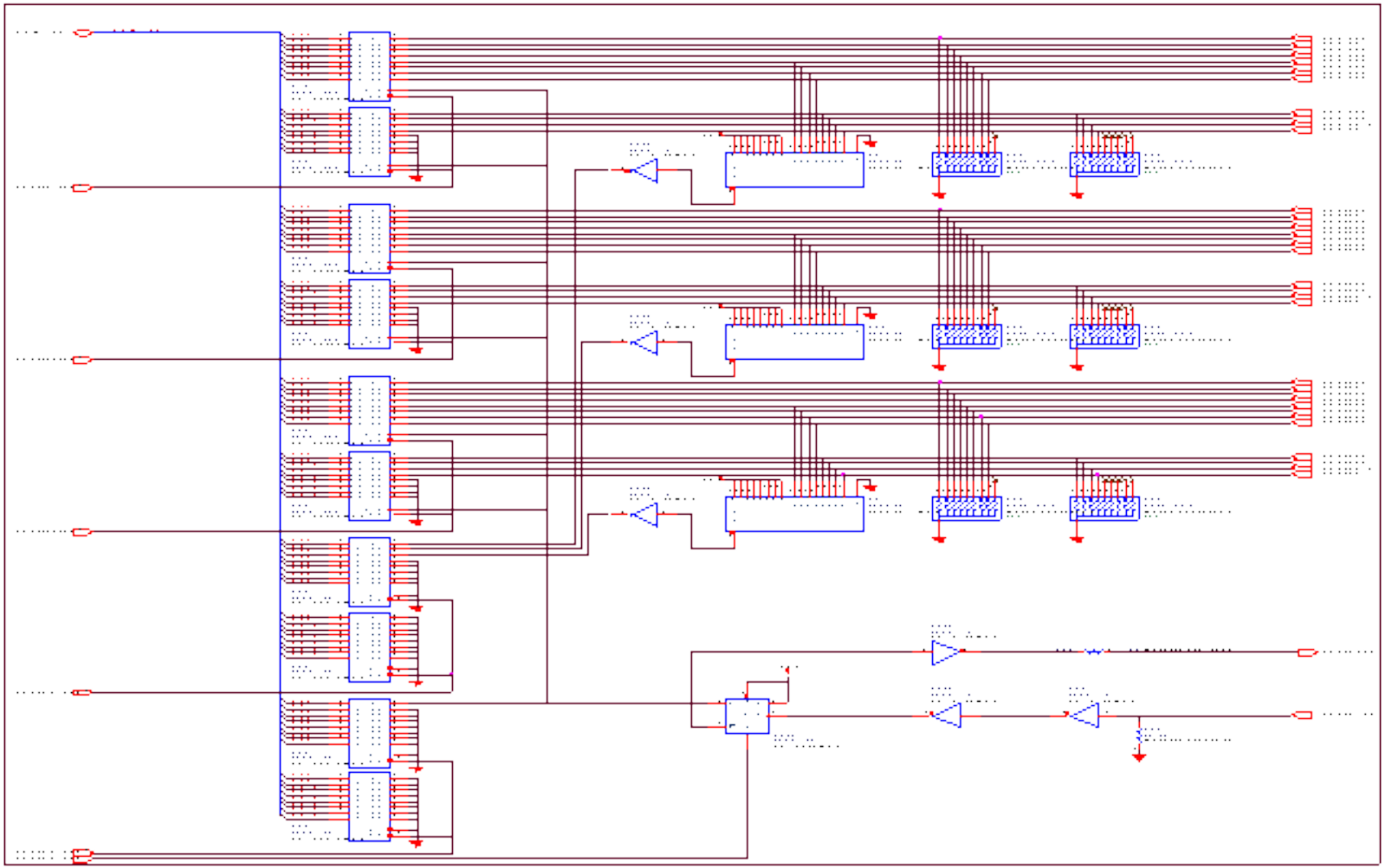
The detector event interface includes event saturation comparators for each of the three 12-bit event words. The detector event saturation flags are read by the DPU microprocessor on a "3-bit" input port which forces the other 13 bits to zero. The additional hardware of the saturation comparators improves DPU throughput by moving a time consuming step in the event processing algorithm from software into hardware.

DPU outputs to the detector electronics are Harris HCTS terminated with 100 ohm resistors.

DPU inputs from the detector electronics are Harris HCTS pulled down with 47 Kohm resistors.

GUVI Detector Processor Hardware

Detector Event Interface



GUVI Detector Processor Hardware

Detector Control Interface

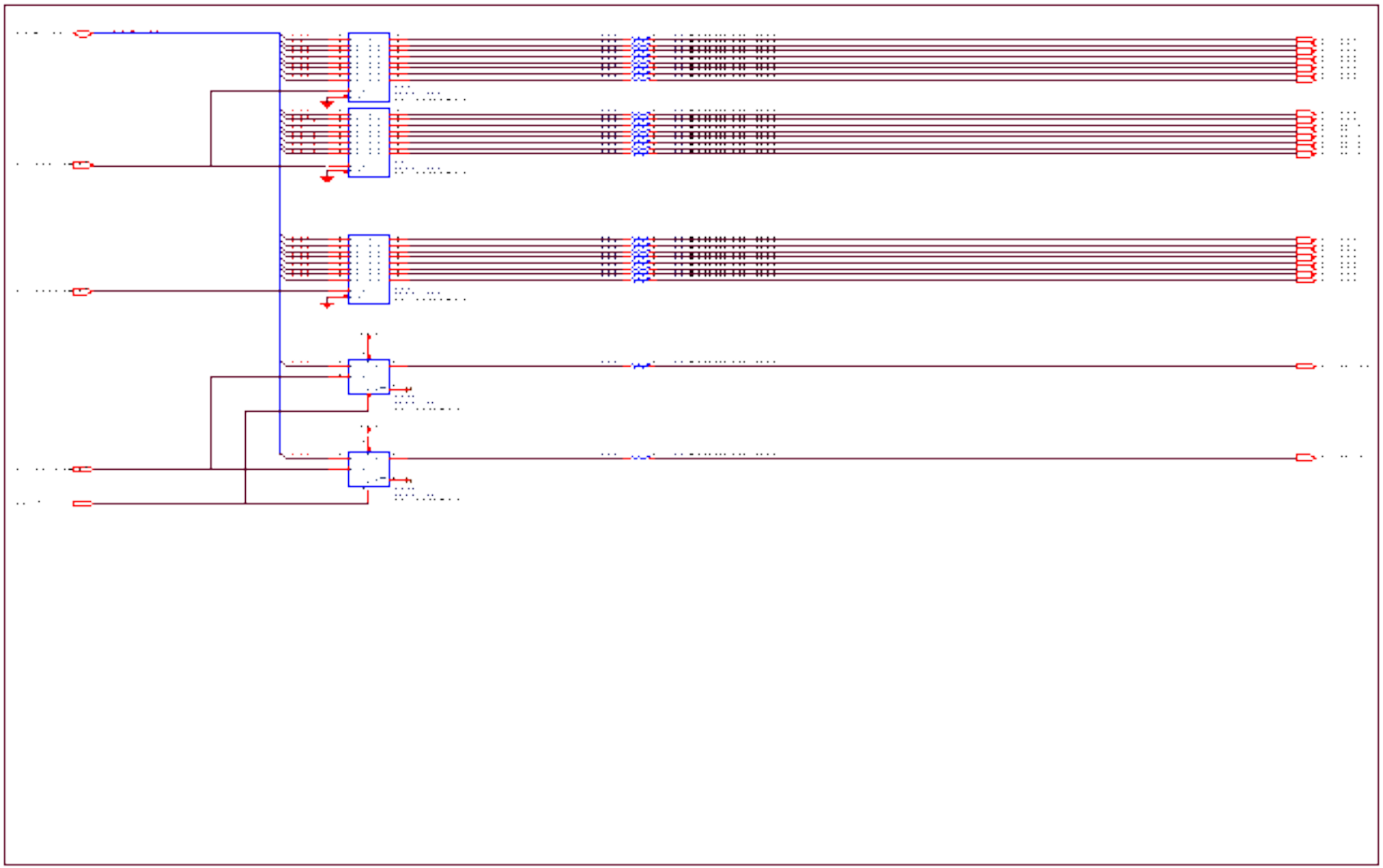
The DPU configures the detector electronics via the detector control interface. The interface consists of a 16-bit parallel output port for data, an 8-bit output port for address and a 2-bit output port for control strobes. All signals on the interface are outputs from the DPU.

The DPU software will control the relative and absolute timing relationships between address, data and control strobes. There are no hardware interlocks.

DPU outputs to the detector electronics are Harris HCTS terminated with 100 ohm resistors.

GUVI Detector Processor Hardware

Detector Control Interface



GUVI Detector Processor Hardware

Telemetry Processor Interface

The DPU communicates with the Telemetry Processor via a pair of 16 bit parallel interfaces.

The DPU data input interface is used to load application software and configure the DPU. The interface is implemented in the DPU as a 16-bit input port with "data ready" and "data acknowledge" handshaking.

The DPU data output interface is used to pass integrated event data to the Telemetry Processor. The interface is implemented in the DPU as a 16-bit output port with "data ready" and "data acknowledge" handshaking.

The Telemetry Processor provides a reset input to the DPU. This reset is OR'ed together with a simple power on reset generated within the DPU. There is now watchdog timer within the DPU since the Telemetry Processor will periodically reset the DPU.

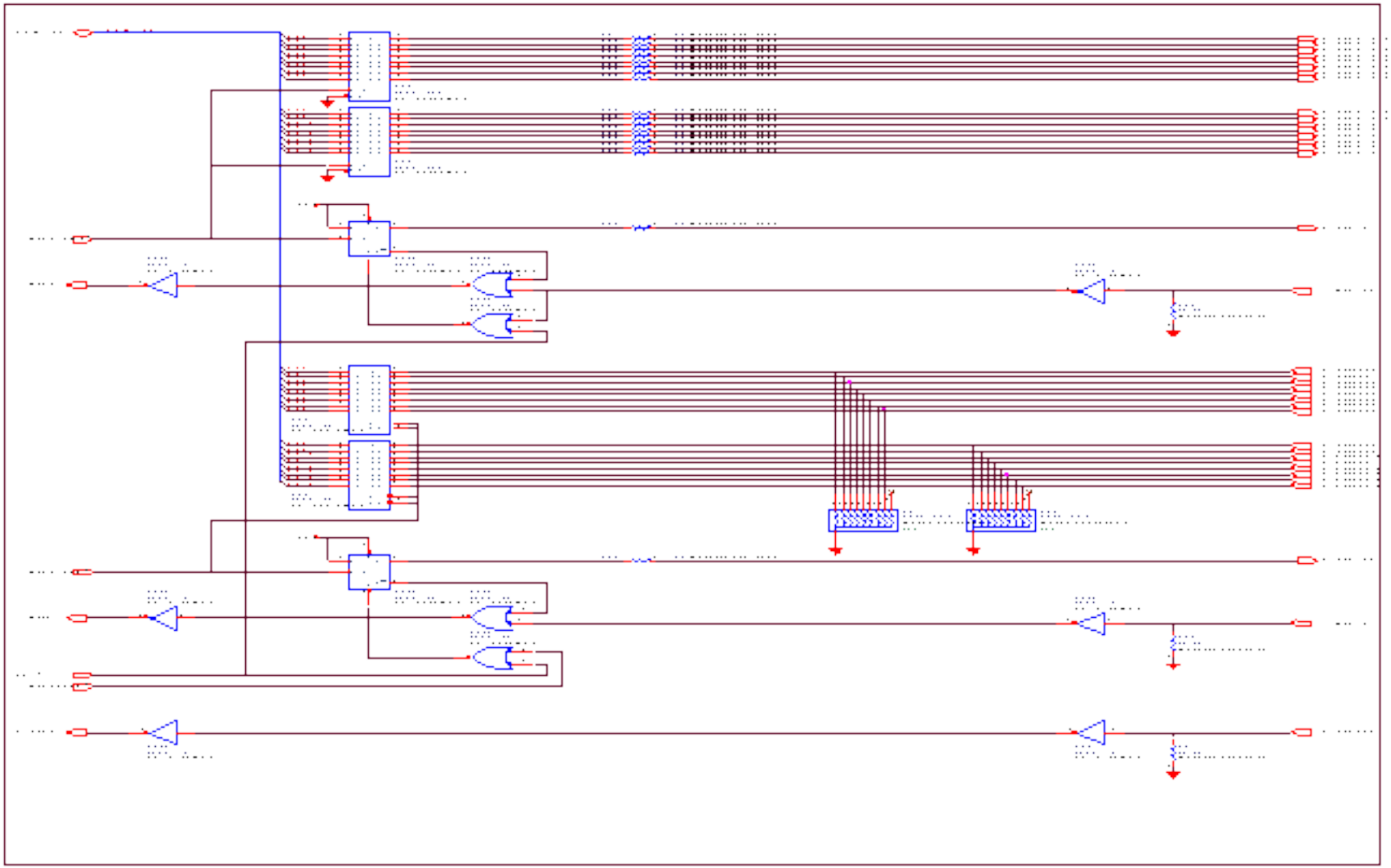
All DPU / Telemetry Processor interface signals travel across the ECU backplane. No external cables are required.

DPU outputs are Harris HCTS terminated with 100 ohm resistors.

DPU inputs are Harris HCTS pulled down with 47.5 Kohm resistors.

GUVI Detector Processor Hardware

Telemetry Processor Interface



GUVI Detector Processor Hardware

Test Equipment Interface

The DPU has two interfaces to ground test equipment to aid in hardware checkout, software development and sensor development. Both interfaces are via "D" connectors that project through openings in the cover of the ECU. The connectors will be capped for flight.

The DPU serial testport is a 9600 baud RS-232 link using a software UART. An adapter unit converts the 5 volt single-ended logic signals used by the DPU to true RS-232 signals for the test equipment computer. A DPU reset input is also available to the test equipment computer. The DPU boot code will support software downloads and debugging via the serial testport.

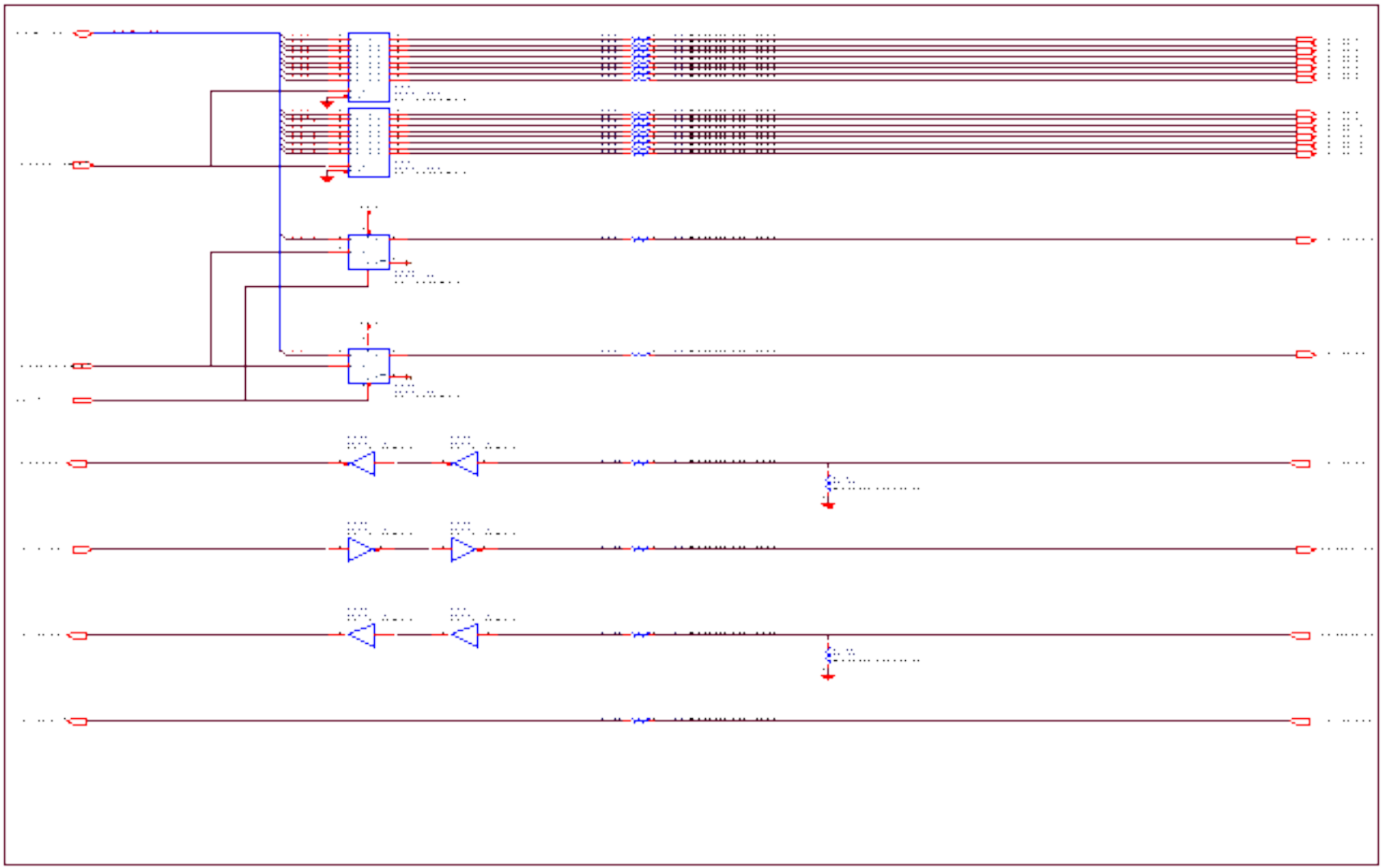
The DPU LabView testport is a 16-bit parallel output port with a pair of data strobe output signals. The interface can be cabled directly to a LabView compatible data acquisition board. During sensor development, the DPU can be programmed to output integrated event data and counter data directly to the test equipment computer bypassing the telemetry processor.

DPU outputs are Harris HCTS terminated with 100 ohm resistors.

DPU inputs are Harris HCTS pulled down with 47.5 Kohm resistors.

GUVI Detector Processor Hardware

Test Equipment Interface



GUVI Detector Processor Hardware

PROM Timing Margins

	Time	Function	Cap Load (pf)	Cap Factor (ns/50 pF)	Length (inches)
Chip Select access	166.7 ns	RIX cycle			
-	72.7 ns	RIX address			
-	0.0 ns	RIX address cap delay	29	5	4
-	12.0 ns	AC139 decode			
-	0.0 ns	AC139 decode cap delay	32	1	4
-	35.0 ns	PROM access			
-	4.7 ns	PROM access cap delay	97	5	8
-	25.0 ns	RIX setup			
	17.3 ns	margin			

	Time	Function	Cap Load (pf)	Cap Factor (ns/50 pF)	Length (inches)
Address access	166.7 ns	RIX cycle			
-	72.7 ns	RIX address			
-	3.7 ns	RIX address cap delay	87	5	8
-	35.0 ns	PROM access			
-	4.7 ns	PROM access cap delay	97	5	8
-	25.0 ns	RIX setup			
	25.6 ns	margin			

	Time	Function	Cap Load (pf)	Cap Factor (ns/50 pF)	Length (inches)
Output Enable access	76.3 ns	RIXPCLK strobe			
-	0.0 ns	RIXPCLK strobe delay	34	5	4
-	10.0 ns	AC139 decode			
-	1.0 ns	AC139 decode cap delay	98	1	8
-	15.0 ns	PROM access			
-	4.7 ns	PROM access cap delay	97	5	8
	25.0 ns	RIX setup			
	20.7 ns	margin			

Assumptions

1. VCC = 4.50 to 5.50 volts
2. Temperature = -55 deg C to +125 deg C
3. Capacitive loads calculated using estimated trace length
4. Capacitive loads calculated using 4 pF/inch measured on NEAR flight board

GUVI Detector Processor Hardware

Accumulator Timing Margins

Chip Select access	Time	Function	Cap Load (pf)	Cap Factor (ns/50 pF)	Length (inches)
	166.7 ns	RIX cycle			
-	72.7 ns	RIX address			
-	0.0 ns	RIX address cap delay	29	5	4
-	12.0 ns	AC139 decode			
-	0.0 ns	AC139 decode cap delay	32	1	4
-	25.0 ns	ASIC access			
-	8.7 ns	ASIC access cap delay	97	5	8
-	25.0 ns	RIX setup			
	23.3 ns	margin			

Address access	Time	Function	Cap Load (pf)	Cap Factor (ns/50 pF)	Length (inches)
	166.7 ns	RIX cycle			
-	72.7 ns	RIX address			
-	3.7 ns	RIX address cap delay	87	5	8
-	25.0 ns	ASIC access			
-	8.7 ns	ASIC access cap delay	97	5	8
-	25.0 ns	RIX setup			
	31.6 ns	margin			

Output Enable access	Time	Function	Cap Load (pf)	Cap Factor (ns/50 pF)	Length (inches)
	76.3 ns	RIXPCLK strobe			
-	0.0 ns	RIXPCLK strobe delay	34	5	4
-	10.0 ns	AC139 decode			
-	1.0 ns	AC139 decode cap delay	98	1	8
-	25.0 ns	ASIC access			
-	8.7 ns	ASIC access cap delay	97	5	8
	25.0 ns	RIX setup			
	6.7 ns	margin			

Assumptions

1. VCC = 4.50 to 5.50 volts
2. Temperature = -55 deg C to +125 deg C
3. Capacitive loads calculated using estimated trace length
4. Capacitive loads calculated using 6 pF/inch measured on NEAR flight board

GUVI Detector Processor Hardware

SRAM Timing Margins

	Time	Function	Cap Load (pf)	Cap Factor (ns/50 pF)	Length (inches)
Chip Select access	166.7 ns	RIX cycle			
-	72.7 ns	RIX address			
-	0.0 ns	RIX address cap delay	29	5	4
-	12.0 ns	AC139 decode			
-	0.0 ns	AC139 decode cap delay	32	1	4
-	40.0 ns	RAM access			
-	4.7 ns	RAM access cap delay	97	5	8
-	25.0 ns	RIX setup			
	12.3 ns	margin			

	Time	Function	Cap Load (pf)	Cap Factor (ns/50 pF)	Length (inches)
Address access	166.7 ns	RIX cycle			
-	72.7 ns	RIX address			
-	3.7 ns	RIX address cap delay	87	5	8
-	40.0 ns	RAM access			
-	4.7 ns	RAM access cap delay	97	5	8
-	25.0 ns	RIX setup			
	20.6 ns	margin			

	Time	Function	Cap Load (pf)	Cap Factor (ns/50 pF)	Length (inches)
Output Enable access	76.3 ns	RIXPCLK strobe			
-	0.0 ns	RIXPCLK strobe delay	34	5	4
-	10.0 ns	AC139 decode			
-	1.0 ns	AC139 decode cap delay	98	1	8
-	15.0 ns	RAM access			
-	4.7 ns	RAM access cap delay	97	5	8
	25.0 ns	RIX setup			
	20.7 ns	margin			

Assumptions

1. VCC = 4.50 to 5.50 volts
2. Temperature = -55 deg C to +125 deg C
3. Capacitive loads calculated using estimated trace length
4. Capacitive loads calculated using 6 pF/inch measured on NEAR flight board

GUVI Detector Processor Hardware

Recent Changes

Replace 54HCTS logic with 54ACTQ logic on the G Bus input and output ports to improve timing margins. This was a direct parts swap without circuit redesign.

Remove logic gate U48C from DPU input TLM Interface to simplify the DPU software polling logic and remove software timing issues.

Duplicate the RTX interrupt input signals E1 – E4 onto the G Bus input port used for the ADC saturation flags. This was required to port an interrupt driven Forth system to the DPU for software development and board testing. (Original design was inherited from SSUSI).

Replace the RTX Boot pin as the signal used for the RS-232 testport transmitter and reallocate the second LabView testport strobe output for that purpose. This was required to port an interrupt driven Forth system to the DPU for software development and board testing. (Original design was inherited from SSUSI).

Change the reset signal to the ACM03 accumulator chip so that it does not reset with the periodic TLM Processor resets of the DPU. The accumulator contents need to be preserved during these resets.

Use accumulators 9 - 16 in the ACM03 accumulator chip as duplicates of accumulators 1 – 8. This will make the full functionality of the ACM03 available to the DPU.