Focal Plane Electronics

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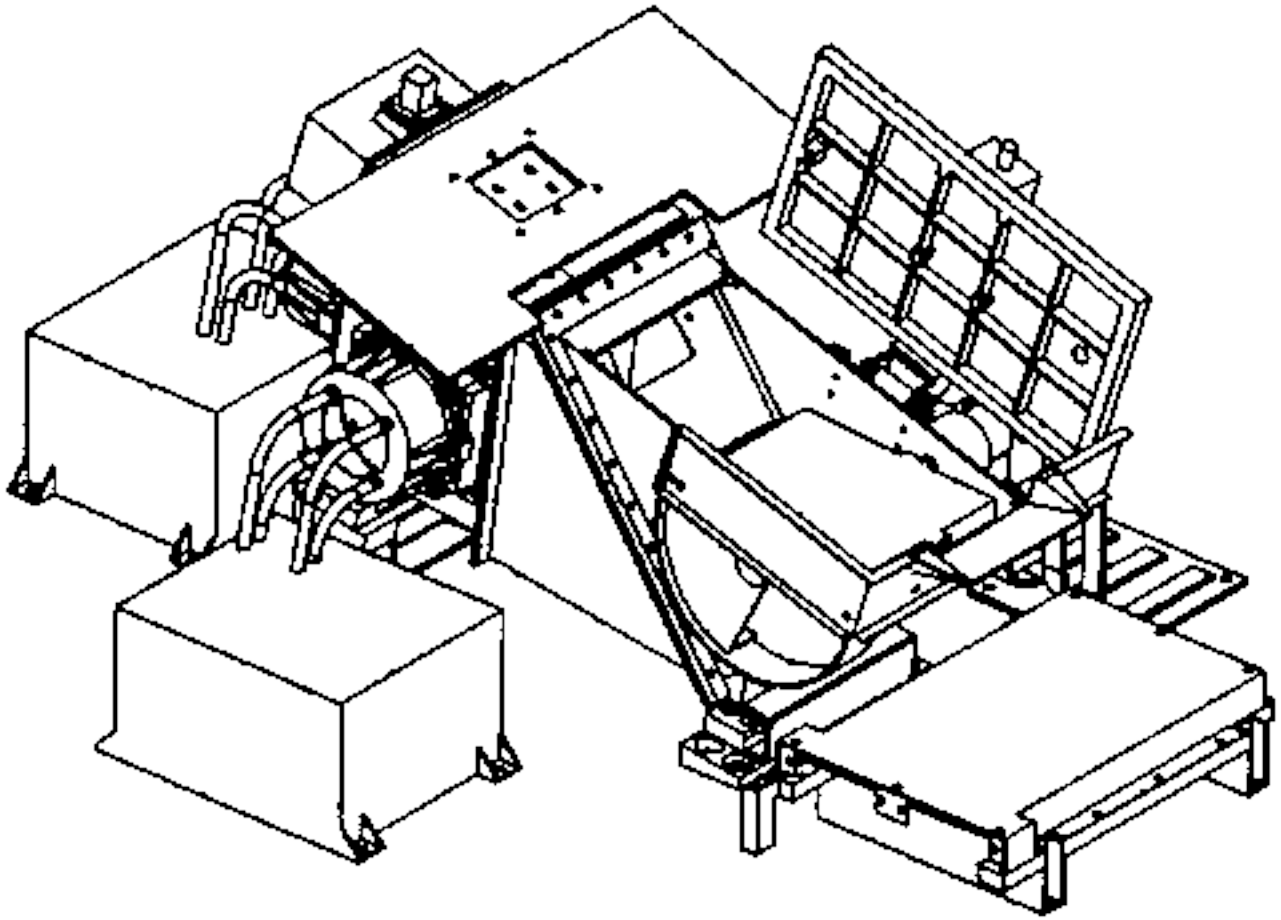
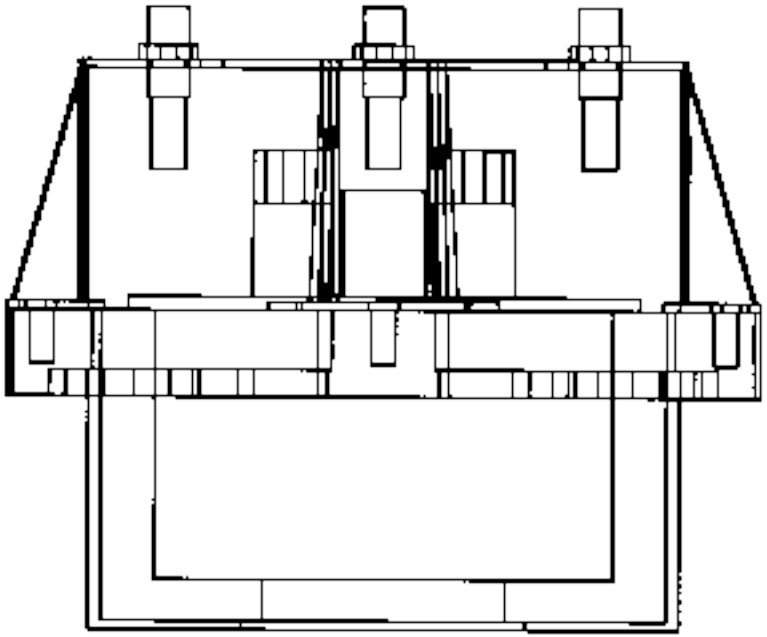
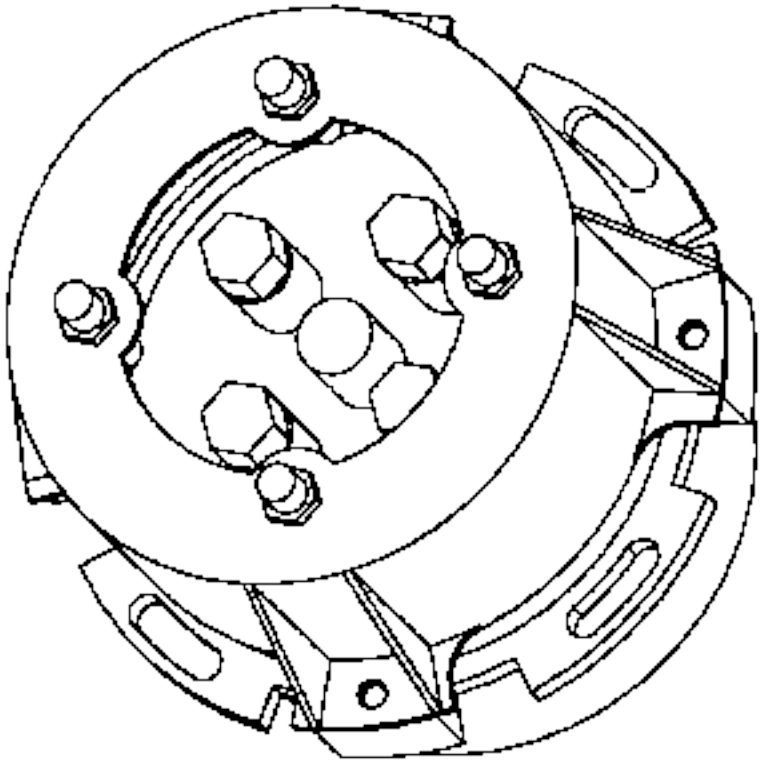
FPE Deck Layout

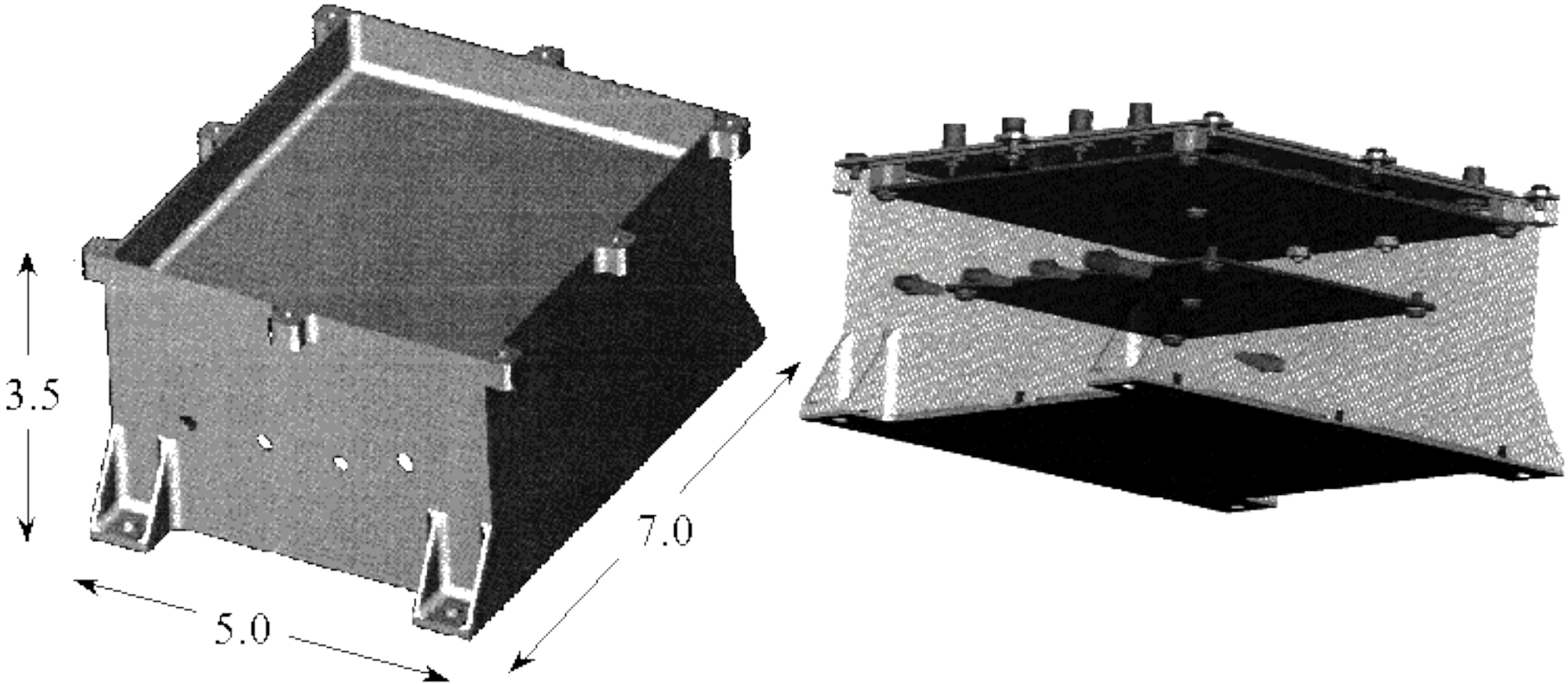


UV Detector Connections



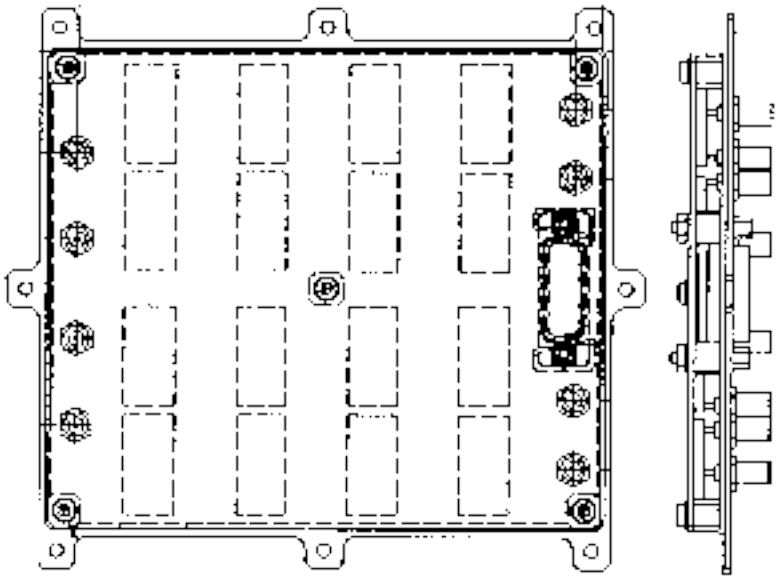


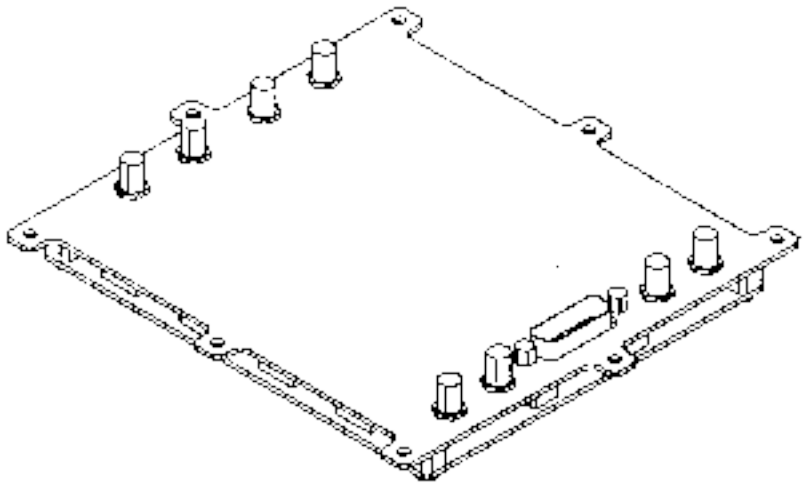
FPE Packaging



all dimensions in inches

Preamp Packaging

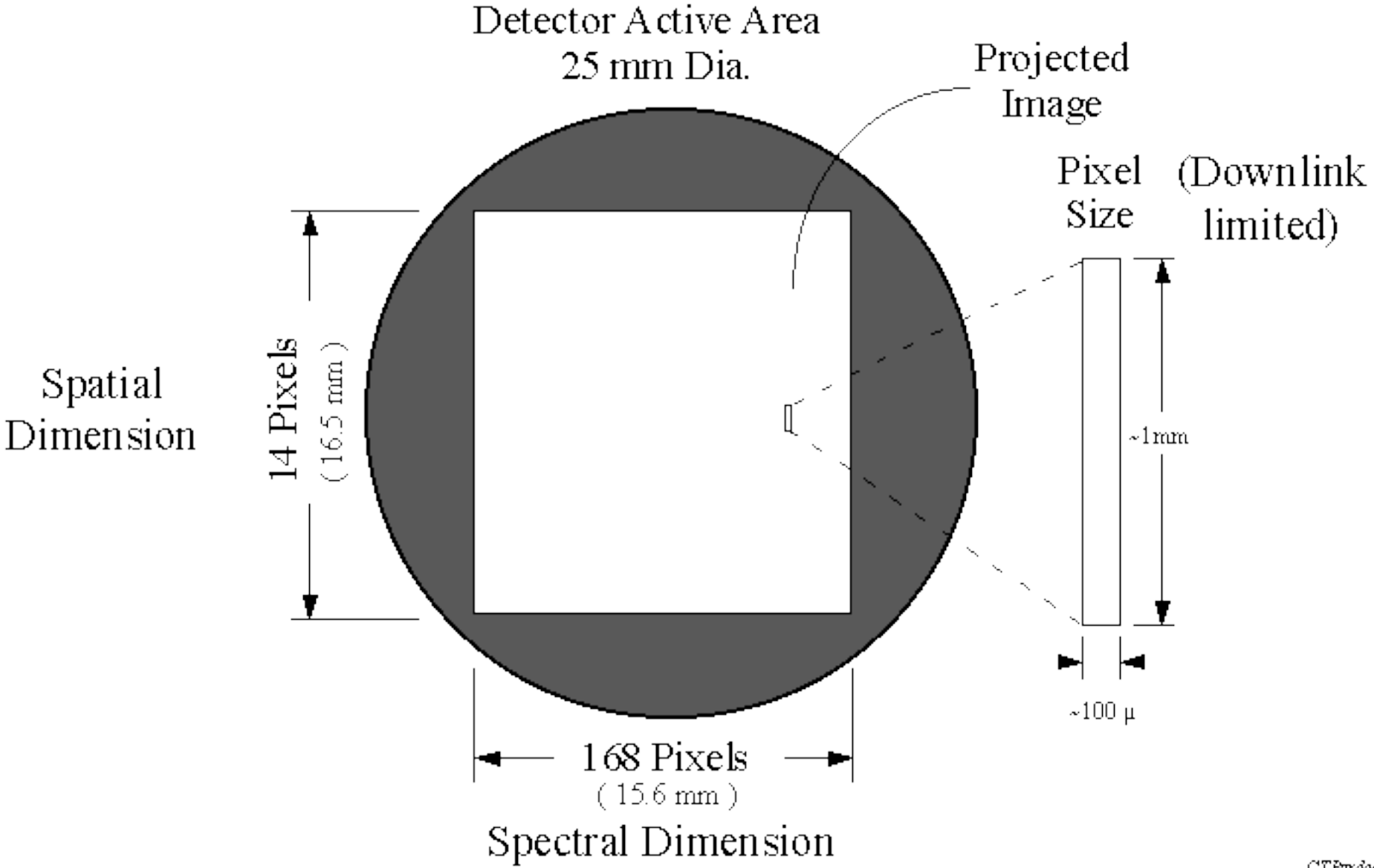




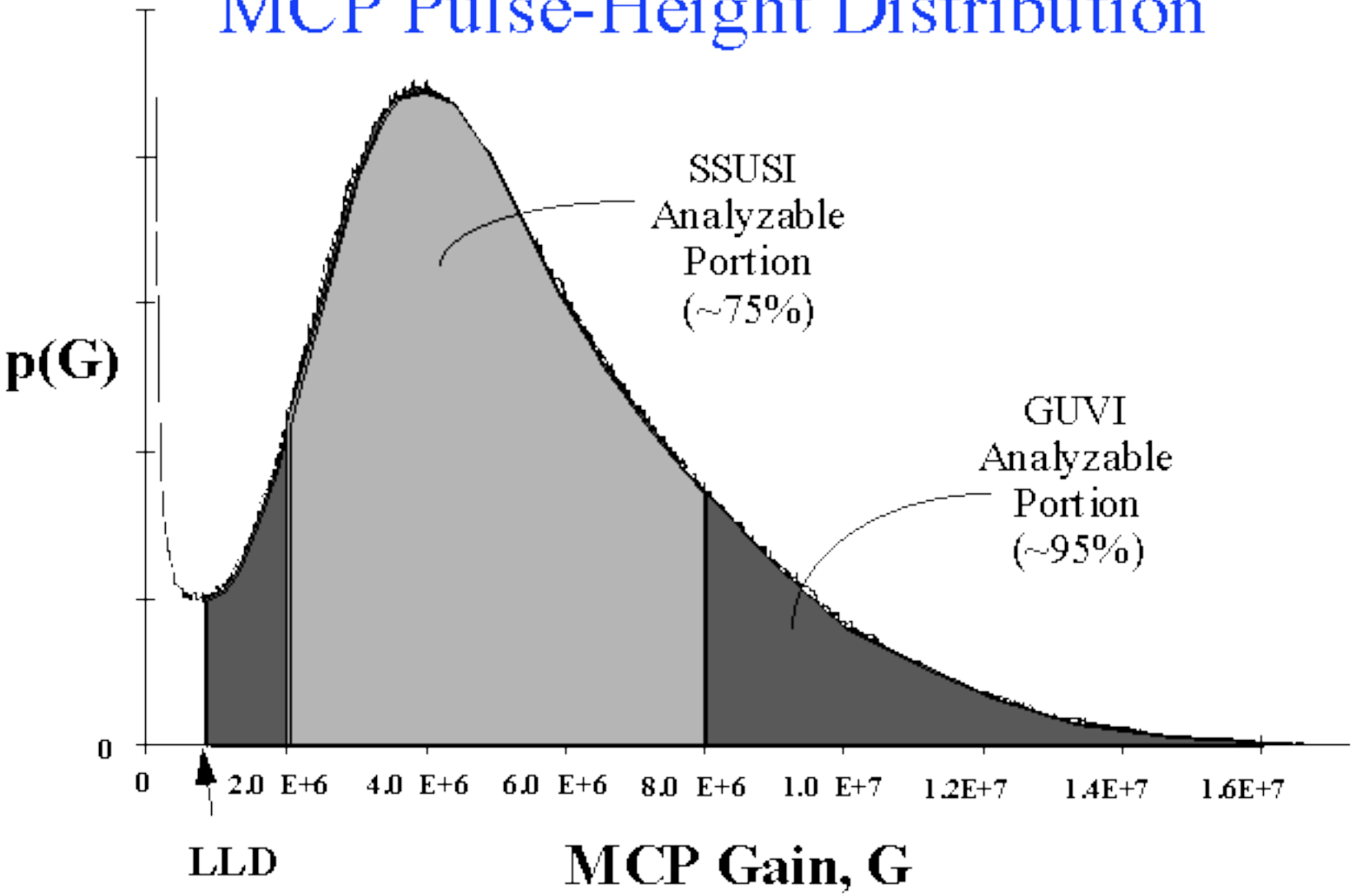
Focal Plane Electronics: Salient Requirements

- Operate at high count rates; > 200 kHz
- Preserve intrascence dynamic range
  - High event throughput (> 70%)
  - Low percentage of mislocated photons (<0.5%)
- Spectral resolution limited by spectrograph optics; not detector system => resolution better than 1nm (225 µm on focal plane)
- Low image distortion (<5%); some post-correction possible
- Image shift vs. count rate held below one pixel
- Long-term stability
  - input rate estimate maintained to better than 10%
  - image drift < 1 pixel

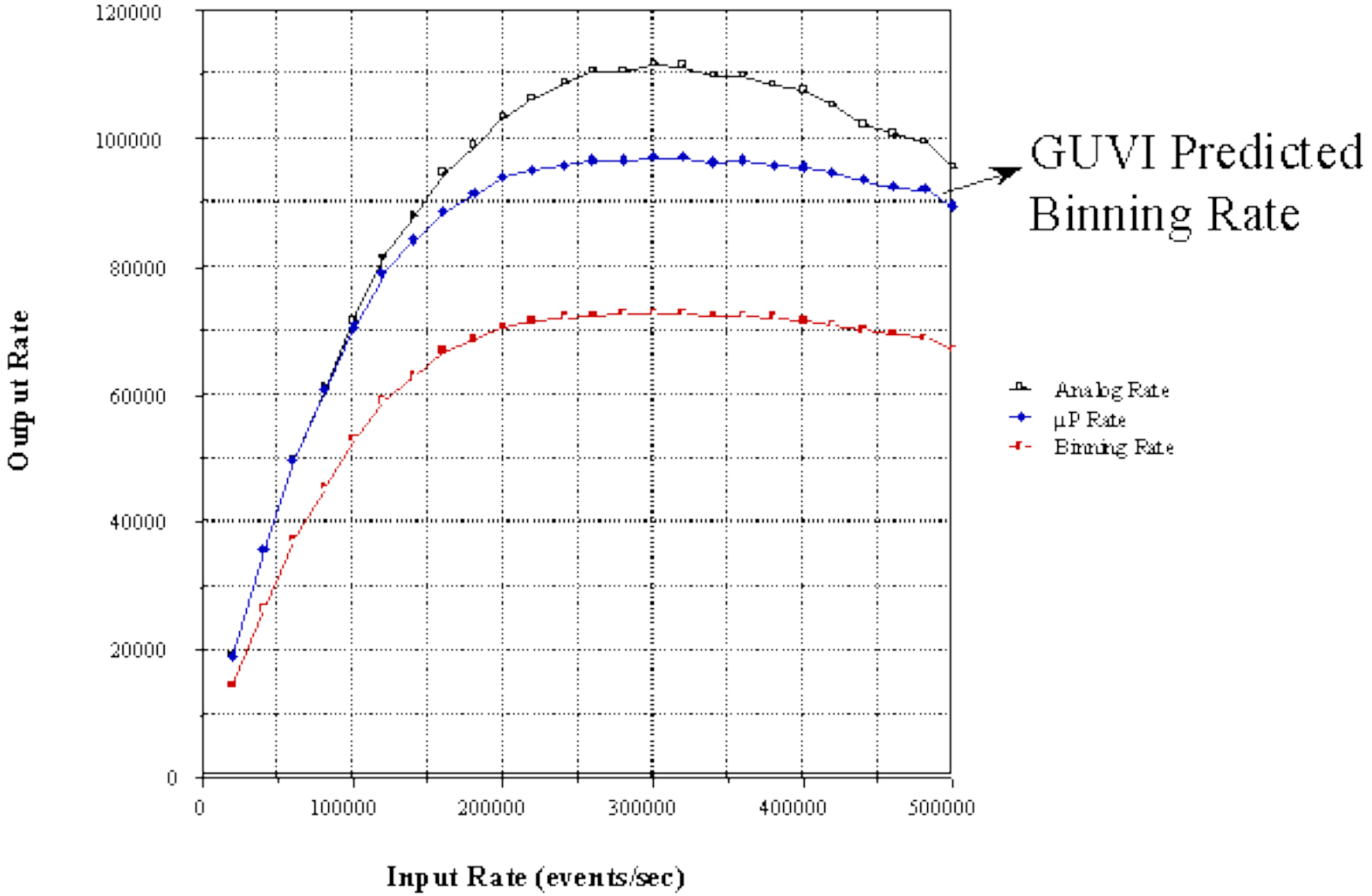
UV Detector - Focal Plane



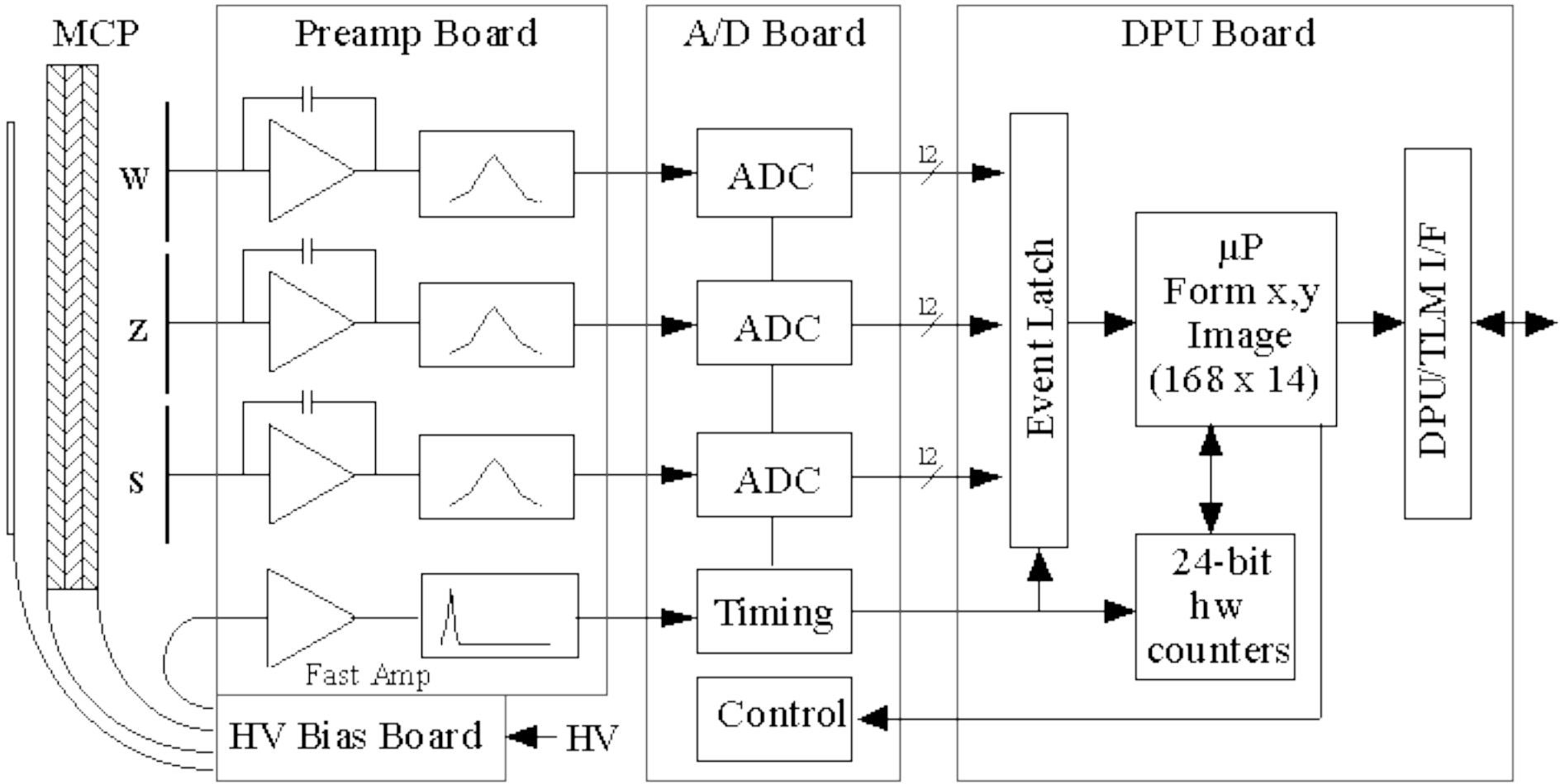
MCP Pulse-Height Distribution



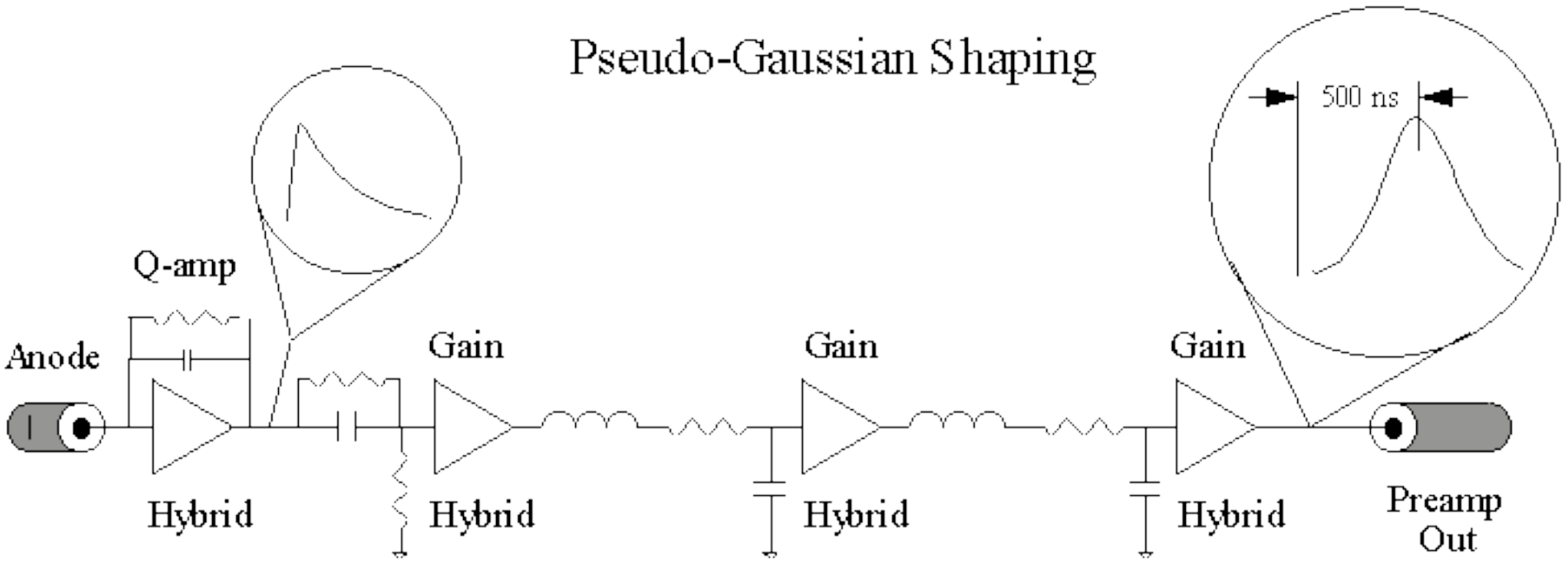
SSUSI Predicted Throughput



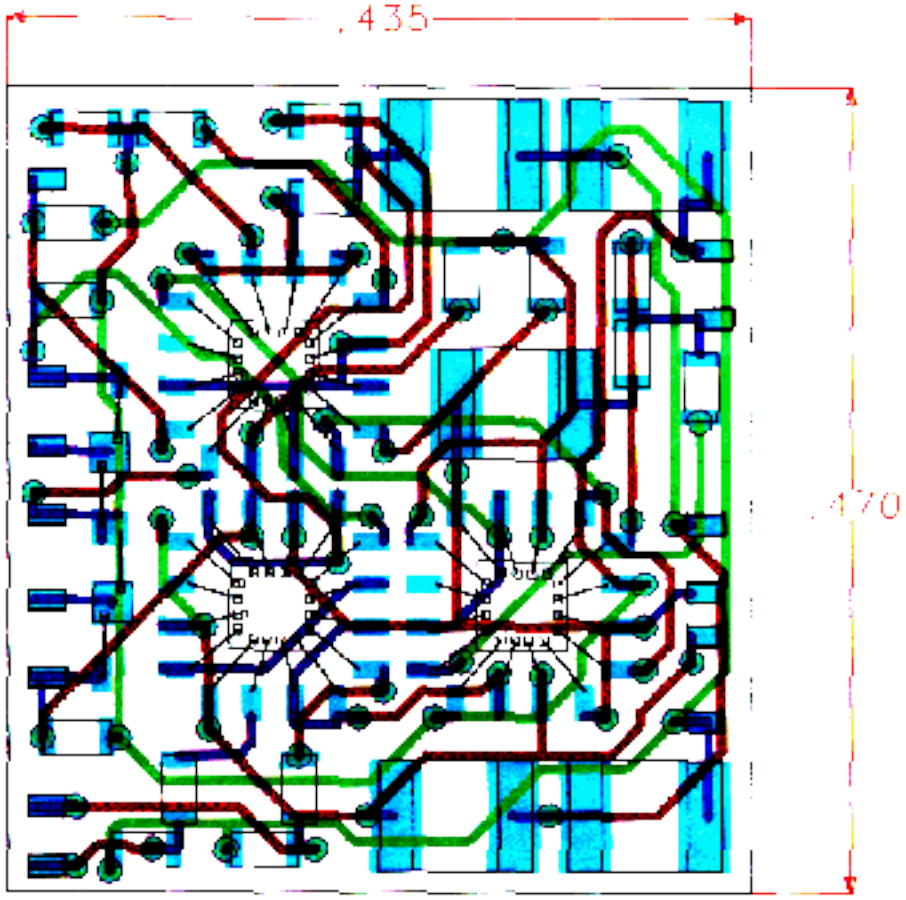
Focal Plane Electronics



Preamplifier/Shaper

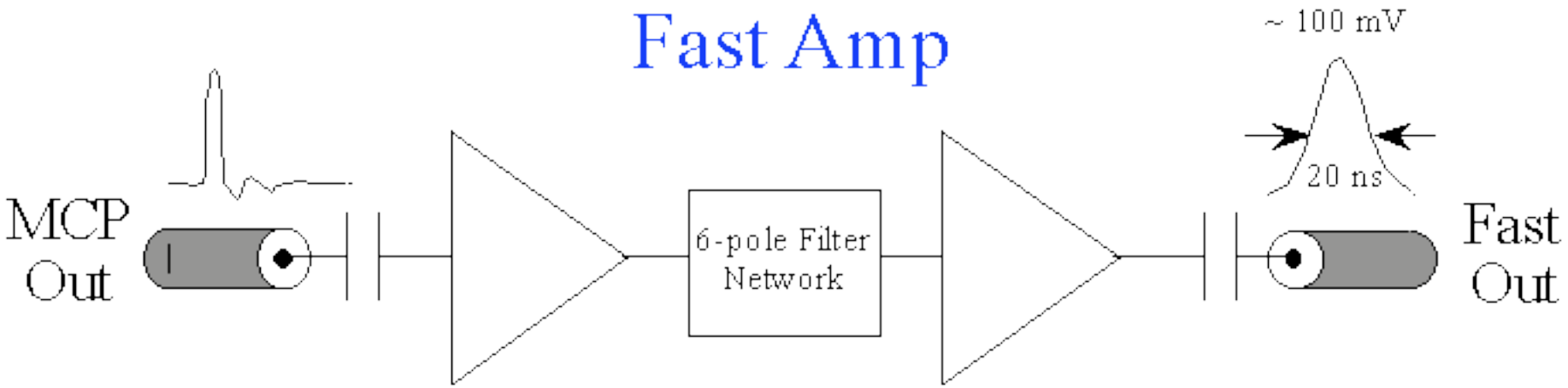


Custom Hybrid



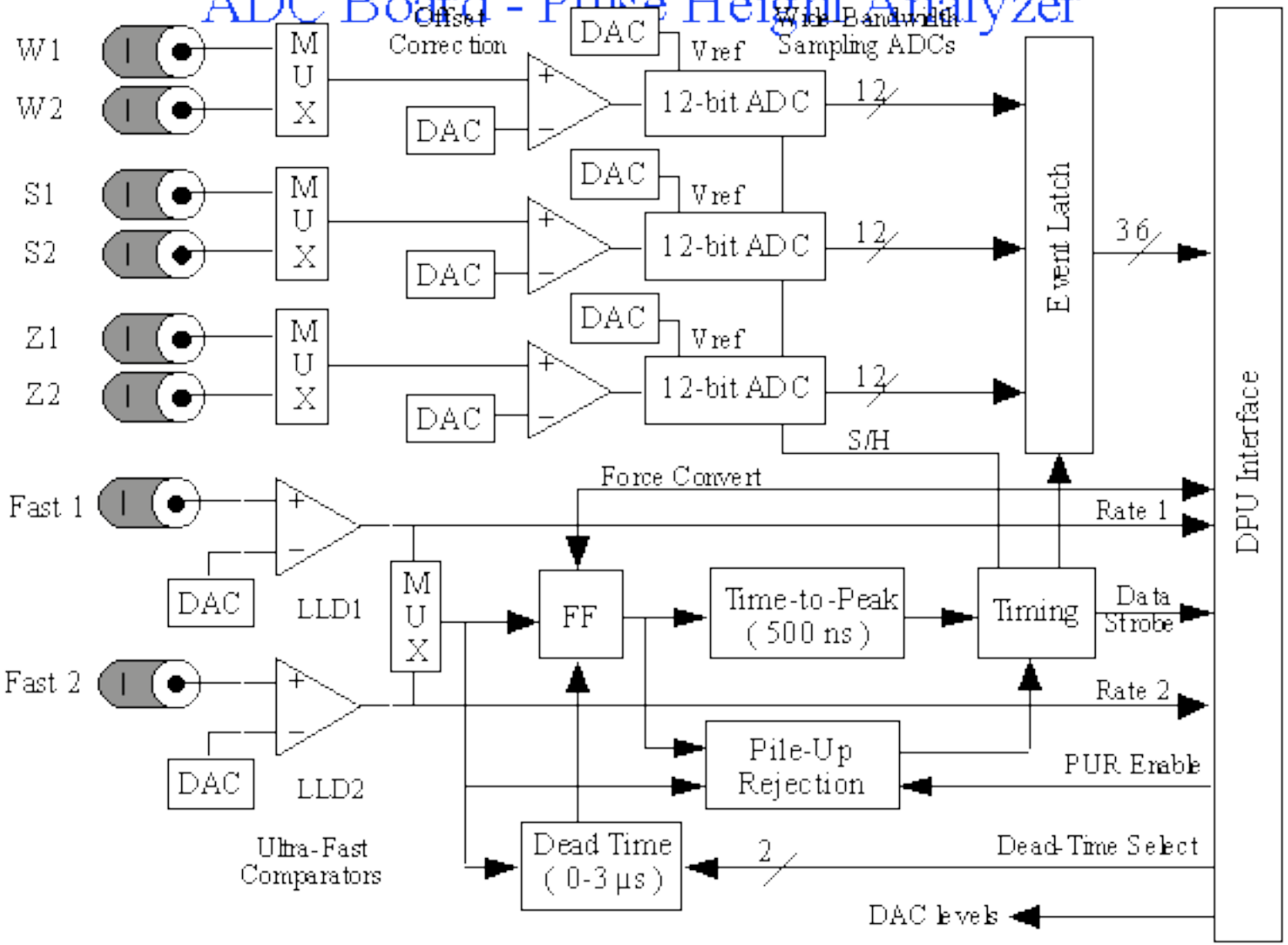
- Fast low-noise Q-amp
  - internal FET (matched-pair)
  - external bias adjustment
  - direct coupling to anode
  - eliminates inter-electrode potentials
- JFET OP-amp
  - low noise 3.6 nV/√Hz
  - GBW 180 MHz (G=3)
  - high slew rate > 150V/µs
  - low power 21mW @ ±5V
  - offset nulling capability

Fast Amp



- Discrete design
  - updated BJTs 8GHz f_T
  - tailorable shaping time 5-20ns
- Low power ~80mW @ ±5V
- Gain stability better than 5% over temp
- Noise ~ 1E4 electrons rms

ADC Board - Pulse Height Analyzer



Detector Data Processing

Poll for new event

Read raw W, S, I A/D values, check bounds

Compute x-y position

$$\text{Spectral coordinate} = \frac{aW}{W+S+I} - \text{offset}_a$$

$$\text{Spatial coordinate} = \frac{bS}{W+S+I} - \text{offset}_b$$

Quantize Results
- 8-bit Spectral
- 5-bit Spatial

Increment Corresponding Memory Bin

Changes Since PDR

Repartioning - Repackaging: Detector

- **Detector bias boards moved to Focal Plane Electronics.**
  - **Simplifies tube assembly; integrated "curved" boards not req'd.**
  - **Allows for improved HV filtering; lower LLD, long term stability.**
  - **All tube connections go to FPE. Location of HVPS not critical.**

Changes Since PDR (cont.)

Repartioning - Repackaging: FPE

- A/D Board moved from FPE to ECU.
  - **One A/D board mux'ed between two detectors. Eliminates 1 board and massive harness.**
  - **Allows increased DPU control of PHA functions.**
  - **Improved performance; 12-bit A/D's, variable gain system, dc offset adjust, and selectable dead-time.**
- Preamp re-design
  - **Custom hybrid; direct coupling to anodes to improve image distortion, resolution, and high count rate performance.**
  - **(3) preamp channels + fast amp together on a single board.**
- Simplified FPE housing
  - **Height compatible with GUVI detector positions.**
  - **No little access covers, strange lips, or semi-rigid cables.**
  - **HV Bias board inside isolated section.**

Changes Since PDR (cont.)

Repartioning - Repackaging: DPU

- Updated design.
  - **Increased memory to allow fast 256 x 256 image binning.**
  - **Hardware rate counters moved to DPU; facilitates stand alone testing.**
  - **Logic to speed up event processing.**
  - **Migration to RTX2010 (SMT SOS part).**
- Digital data transfer from A/D Board over backplane
  - **Eliminates massive harness.**
  - **Accommodates additional PHA controls.**
  - **Incorporates new I/O interface to TLM processor**

Focal Plane Image Accumulation